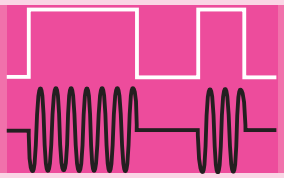
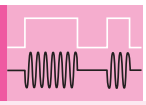
PART TWO

DIGITAL ELECTRONICS



CHAPTER 6



INTRODUCTION TO DIGITAL ELECTRONICS

Chapter Outline

Chapter Goals

- Introduce binary digital logic concepts
- Explore the voltage transfer characteristics of ideal and nonideal inverters
- Define logic levels and logic states at the input and output of logic gates
- Present goals for logic gate design
- Understand the need for noise rejection and the concept of noise margin
- Introduce measures of dynamic performance of logic gates including rise time, fall time, propagation delay, and power-delay product
- Review Boolean algebra and the NOT, OR, AND, NOR, and NAND functions
- Explore simple transistor implementations of the inverter
- Introduce diode logic and diode-transistor logic circuits
- Explore the design of MOS logic gates employing single transistor types — either NMOS or PMOS transistors (known as single-channel technology)
- Learn basic inverter design; discover why transistors are used in place of resistors
- Understand design and performance differences between saturated load, linear load, and depletion-mode load circuits
- Present examples of noise margin calculations
- Learn to design multiinput NAND and NOR gates
- Learn to design complex logic gates including sum-of-products representations
- Develop expressions and approximation techniques for calculating rise time, fall time, and propagation delay of the various single-channel logic families

Digital electronics has had a profound effect on our lives through the pervasive application of microprocessors and microcontrollers in consumer and industrial products. The microprocessor chip forms the heart of personal computers and workstations, and digital signal processing is the basis of modern telecommunications. Microcontrollers are found in everything from CD/MP3 players to refrigerators to washing machines to vacuum cleaners, and in today's luxury automobiles often more than 50 microprocessors work together to control the vehicle. In fact, as much as 40 to 50 percent of the total cost of luxury cars is projected to come from electronics in the near future.

The digital electronics market is dominated by far by **complementary MOS,** or **CMOS, technology.** However, as pointed out in previous chapters, the first successful manufacturing processes were developed for bipolar devices and the first integrated circuits utilized bipolar transistors. The rapid advance in the application of digital electronics was facilitated by circuit designers who developed early bipolar logic families called resistor-transistor logic (RTL) and

Intel Founders Andy Grove, Robert Noyce, and Gordon Moore with rubylith layout of 8080 microprocessor.
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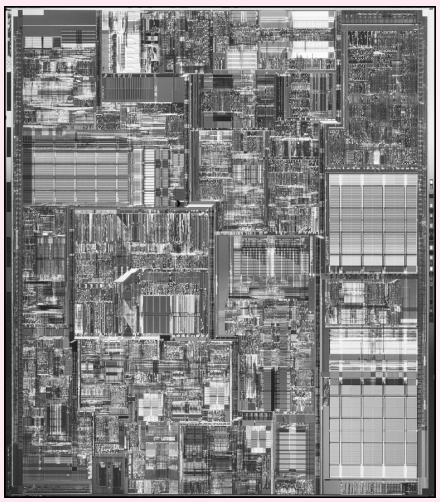


Intel IA-64 Microprocessor employing more than 25M transistors.
Photo Courtesy of Intel Corporation

diode-transistor logic (DTL). These families were subsequently replaced with highly robust bipolar logic families including **transistor-transistor logic (TTL)** and **emitter-coupled logic (ECL)** that could be easily interconnected to form highly reliable digital systems. High-performance forms of TTL and ECL remain in use today.

It took almost a decade to develop viable MOS manufacturing processes. The first high-density MOS integrated circuits utilizing PMOS technology appeared around 1970. The landmark development of the microprocessor is attributed to Ted Hoff who convinced Intel to develop the 4-bit 4004 microprocessor chip containing approximately of 2300 transistors that was introduced in 1971.

As with many advances, work on single-chip processors started rapidly in research and development laboratories around the world. In the following 30 years, the industry went on to develop microprocessor chips of incredible complexity. As this edition is written, the IA-64 chip employing more than 25 million transistors has been introduced, and the ITRS projections in Chapter 1 predict microprocessors with more than a billion transistors will appear by the year 2010.

By the mid 1970s, PMOS was being rapidly replaced by the higher-performance NMOS technology. The Intel 8080, 8085, and 8086 were all implemented in NMOS logic. A significant advance in NMOS circuit performance was achieved with the introduction of the depletion-mode load device, and this work was formally recognized when Dr. Toshiaki Masuhara of Hitachi received the 1990 IEEE Solid-State Circuits Technical Field Award for this work.

But by the mid 1980s, power dissipation levels associated with NMOS microprocessors had reached unmanagable levels, and the industry made a transition to CMOS technology almost overnight. CMOS has remained the dominant technology since that time.

In this chapter, we begin our study of digital logic circuits with the introduction of a number of important concepts and definitions related to logic circuits. Then the chapter looks in detail at the design of MOS logic circuits built using only a single transistor type — either NMOS or PMOS — referred to as "single-channel technology." Complementary MOS (CMOS) logic, that uses both NMOS and PMOS transistors, is discussed in Chapter 7, and MOS memory and storage circuits are introduced in Chapter 8. Bipolar logic circuits are discussed in Chapter 9.

This chapter explores the requirements and general characteristics of digital logic gates. Subsequent chapters investigate the detailed implementation of logic gates in both MOS and bipolar technologies. The initial discussion in this chapter focuses on the characteristics of the inverter. Important logic levels associated with binary logic are defined, and the concepts of the voltage transfer characteristic and noise margin are introduced. Later, the temporal behavior and time delays of the gates are addressed. A review of Boolean algebra, used for representation and analysis of logic functions, is included, and simple AND gates, OR gates, and NAND gates are implemented using diode logic and bipolar transistors.

6.1 IDEAL LOGIC GATES

We begin our discussion of logic gates by considering the characteristics of the ideal logical inverter. Although we cannot achieve the ideal behavior, the concepts and definitions form the basis for our study of actual circuit implementations of MOS and bipolar logic families in Chapters 7, 8, and 9.

In the discussions in this book, we limit consideration to binary logic, which requires only two discrete states for operation. In addition, the positive logic convention will be used throughout: The higher voltage level will correspond to a logic 1, and the lower voltage level will correspond to a logic 0.

The logic symbol and **voltage transfer characteristic (VTC)** for an ideal inverter are given in Fig. 6.1. The positive and negative power supplies, shown explicitly as V_+ and V_-, respectively, are not included in most logic diagrams. For input voltages v_I below the **reference voltage V_{REF},** the output v_o will be in the **high logic level at the gate output V_H.** As the input voltage increases and exceeds V_{REF}, the output voltage changes abruptly to the **low logic level at the gate output V_L.** The output voltages corresponding to V_H and V_L generally fall between the supply voltages V_+ and V_- but may not be equal to either voltage. For an input equal to V_+ or V_-, the output does not necessarily reach either V_- or V_+. The actual levels depend on the individual logic family, and the reference voltage V_{REF} is determined by the internal circuitry of the gate.

In most digital designs, the power supply voltage is predetermined either by technology constraints or system-level power supply criteria. For example, $V_+ = 5.0$ V (with $V_- = 0$) represented

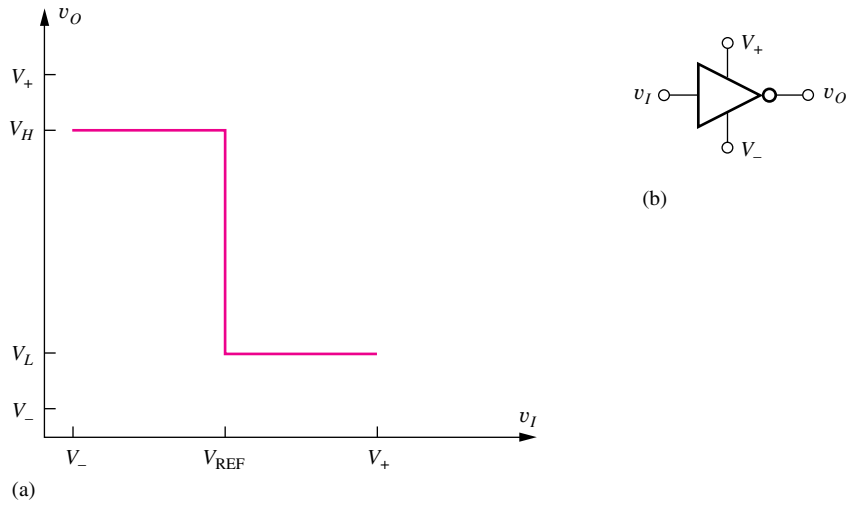


Figure 6.1 (a) Voltage transfer characteristic for an ideal inverter. (b) Inverter logic symbol.

the standard power supply for logic for many years. However, because of the power-dissipation, heat-removal, and breakdown-voltage limitations of advanced technology, a new power supply voltage equal to 3.3 V is in widespread use. In addition, many low-power systems must be designed to operate from battery voltages as low as 1.0 to 1.5 V, and many ICs now operate from supply voltages of 1.8 to 2.5 V.

6.2 LOGIC LEVEL DEFINITIONS AND NOISE MARGINS

Now, let us look at electronic implementations of the inverter. Conceptually, the basic inverter circuit consists of a load resistor and a switch controlled by the input voltage v_I, as indicated in Fig. 6.2(b). When closed, the switch forces v_O to V_L, and when open, the resistor sets the output to V_H. In Fig. 6.2(b), for example, $V_L = 0$ V and $V_H = V_+$.

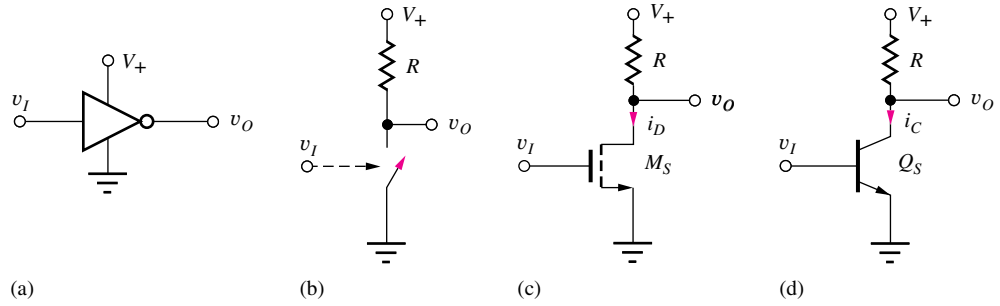


Figure 6.2 (a) Inverter operating with power supplies of 0 V and V_+. (b) Simple inverter circuit comprising a load resistor and switch. (c) Inverter with NMOS transistor switch. (d) Inverter with BJT switch.

The voltage-controlled switch can be realized by either the MOS transistor in Fig. 6.2(c) or the bipolar transistor in Fig. 6.2(d). Transistors M_S and Q_S switch between two states: nonconducting or "off," and conducting or "on". Load resistor R sets the output voltage to $V_H = V_+$ when switching transistor M_S or Q_S is off. If the input voltage exceeds the threshold voltage of M_S or the turn-on voltage of the base-emitter junction of Q_S, the transistors conduct a current that causes the output voltage to drop to V_L. When transistors are used as switches, as in Figs. 6.2(c) and (d), $V_L \neq 0$ V. Detailed discussion of the design of these circuits appears later in this chapter and in Chapter 9.

In the inverter circuit, the transition between V_H and V_L does not occur in the abrupt manner indicated in Fig. 6.1 but is more gradual, as indicated by the more realistic transfer characteristic shown in Fig. 6.3(a). A single, well-defined value of V_{REF} does not exist. Instead, several additional input voltage levels are important.

When the input v_I is below the **input low-logic-level V_{IL},** the output is defined to be in the high-output or 1 state. As the input voltage increases, the output voltage v_o falls until it reaches the low output or 0 state as v_I exceeds the voltage of the **input high-logic-level V_{IH}.** The input voltages V_{IL} and V_{IH} are defined by the points at which the slope of the voltage transfer characteristic equals -1. Voltages below V_{IL} are reliably recognized as logic 0s at the input of a logic gate, and voltages above V_{IH} are recognized reliably as logic 1s at the input. Voltages corresponding to the region between V_{IL} and V_{IH} do not represent valid logic input levels and generate logically indeterminate output voltages. The transition region of high negative slope between these two points[1] represents an undefined logic state. The voltages labeled as V_{OL} and

[1] This region corresponds to a region of relatively high voltage gain. See Probs. 6.6 and 6.7.

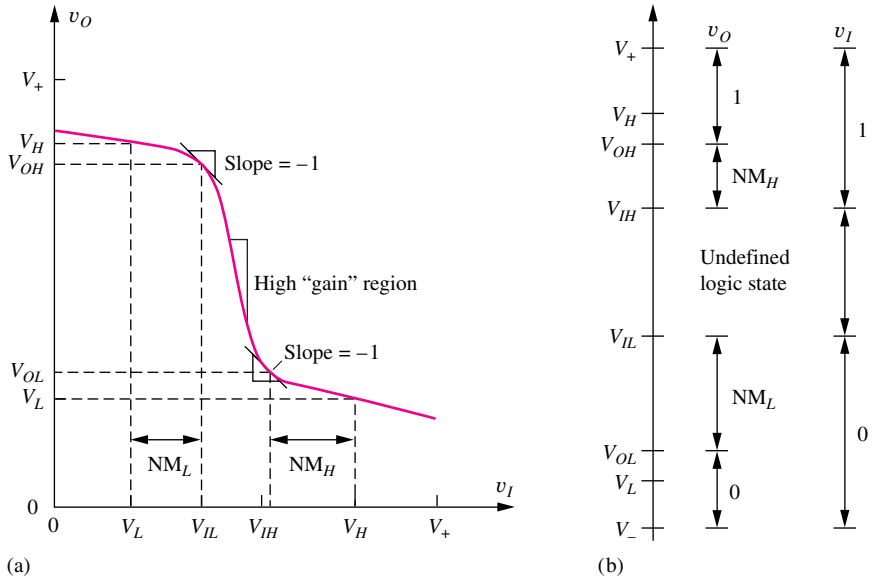


Figure 6.3 (a) Voltage transfer characteristic for the inverters in Fig. 6.2 with $V_- = 0$. (b) Voltage levels and logic state relationships for positive logic.

V_{OH} represent the gate output voltages at the -1 slope points and correspond to input levels of V_{IH} and V_{IL}, respectively.

In Part III of this book, we will find that the region of the VTC with a high negative slope between V_{IL} and V_{IH} corresponds to a large "voltage gain," and we actually use this region for amplification of analog signals. The gain is the slope of the voltage transfer characteristic. The higher the gain, the narrower will be the voltage range corresponding to the undefined logic state in Fig. 6.3.

An alternate representation of the voltages and voltage ranges appears in Fig. 6.3(b), along with quantities that represent the voltage noise margins. The various terms are defined more fully next.

6.2.1 Logic Voltage Levels

V_L The nominal voltage corresponding to a low-logic state at the output of a logic gate for $v_I = V_H$. Generally, $V_- \le V_L$.

V_H The nominal voltage corresponding to a high-logic state at the output of a logic gate for $v_I = V_L$. Generally, $V_H \le V_+$.

V_{IL} The maximum input voltage that will be recognized as a low input logic level.

V_{IH} The minimum input voltage that will be recognized as a high input logic level.

V_{OH} The output voltage corresponding to an input voltage of V_{IL}.

V_{OL} The output voltage corresponding to an input voltage of V_{IH}.

For subsequent discussions of MOS logic, V_- will usually be taken to be 0 V, and V_+ will be either 3.3 V or 5 V. These voltages are also commonly used in bipolar logic. However, other values are possible. For example, emitter-coupled logic, discussed in Chapter 9 on bipolar logic design, has historically used $V_+ = 0$ V and $V_- = -5.2$ V or -4.5 V, and new low-power ECL gates have been developed to operate with a total supply voltage span of only 2 V.

6.2.2 Noise Margins

The **noise margin in the high state NM_H** and **noise margin in the low state NM_L** represent "safety margins" that prevent the gate from producing erroneous logic decisions in the presence of noise sources. The noise margins are needed to absorb voltage differences that may arise between the outputs and inputs of various logic gates due to a variety of sources. These may be extraneous signals coupled into the gates or simply parameter variations between gates in a logic family.

Figure 6.4 shows several interconnected inverters and illustrates why noise margin is important. The signal and power interconnections on a printed circuit board or integrated circuit, which we most often draw as zero resistance wires (or short circuits), really consist of distributed *RLC* networks. In Fig. 6.4 the output of the first inverter, v_{O1}, and the input of the second inverter, v_{I2}, are not necessarily equal. As logic signals propagate from one logic gate to the next, their characteristics become degraded by the resistance, inductance, and capacitance of the interconnections. Rapidly switching signals may induce transient voltages and currents directly onto nearby signal nodes and lines through capacitive and inductive coupling indicated by C_c and M. In an RF environment, the interconnections may even act as small antennae that can couple additional extraneous signals into the logic circuitry. Similar problems occur in the power distribution network. Both direct current and transient currents during gate switching generate voltage drops across the various components (R_p, L_p, C_p) of the power distribution network.

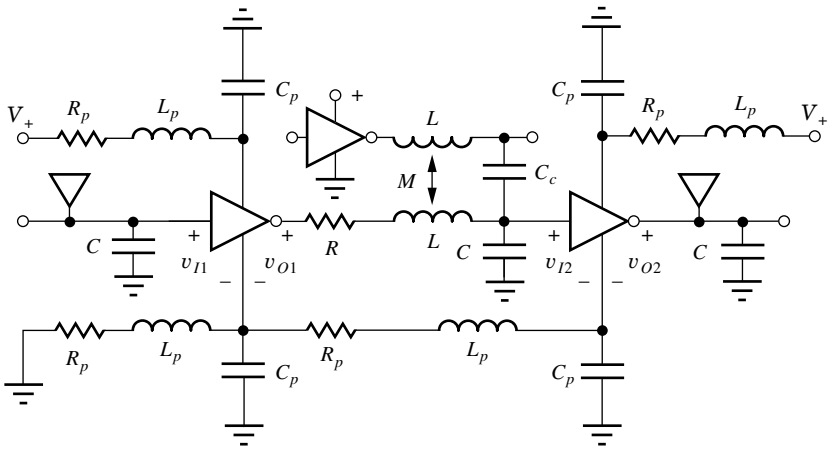


Figure 6.4 Inverters embedded in a signal and power and distribution network.

There are a number of different ways to define the noise margin [1–3] of a logic gate. In this text, we will use a definition based on the input and output voltages at the -1 slope points on the inverter voltage transfer characteristic, as identified in Fig. 6.3:

NM_L The noise margin associated with a low input level is defined by

$$NM_L = V_{IL} - V_{OL} \tag{6.1}$$

NM_H The noise margin associated with a high input level is defined by

$$NM_H = V_{OH} - V_{IH} \tag{6.2}$$

The noise margins represent the voltages necessary to upset the logic levels in a long chain (actually an infinite chain) of inverters, or in the cross-coupled flip-flop storage elements that we explore in Chapter 8. The definitions in Eqs. (6.1) and (6.2) can be shown [1–3] to maximize the sum of

the two noise margins.[2] These definitions provide a reasonable metric for comparing the noise margins of different logic families and are relatively easy to understand and calculate. The method for actually finding the worst-case noise margins for a logic family uses a graphical approach described in [1]. However, it is much more cumbersome to describe and difficult to implement.

The noise margins also help absorb parameter variations that occur between individual logic gates. During manufacture, there will be unavoidable variations in device and circuit parameters, and variations will occur in the power supply voltages and operating temperature during application of the logic circuits. Normally, the logic manufacturer specifies worst-case values for V_H, V_L, V_{IL}, V_{OL}, V_{IH}, and V_{OH}. In our analysis, however, we will generally restrict ourselves to finding nominal values of these voltages.

EXERCISE: A certain TTL gate has the following values for its logic levels: $V_{OH} = 3.6$ V, $V_{OL} = 0.4$ V, $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V. What are the noise margins for this TTL gate?

ANSWERS: $NM_H = 1.6$ V; $NM_L = 0.4$ V

6.2.3 Logic Gate Design Goals

As we explore the design of logic gates, we should keep in mind a number of goals.

1. From Fig. 6.1, we see that the ideal logic gate is a highly nonlinear device that attempts to quantize the input signal into two discrete output levels. In the actual gate in Figs. 6.2 and 6.3, we should strive to minimize the width of the undefined input voltage range, and the noise margins should generally be as large as possible.
2. Logic gates should be unidirectional in nature. The input should control the output to produce a well-defined logic function. Voltage changes at the output of a gate should not affect the input side of the circuit.
3. The logic levels must be regenerated as the signal passes through the gate. In other words, the voltage levels at the output of one gate must be compatible with the input voltage levels of the same or similar logic gates.
4. The output of one gate should also be capable of driving the inputs of more than one gate. The number of inputs that can be driven by the output of a logic gate is called the **fan-out** capability of that gate. The term **fan in** refers to the number of input signals that may be applied to the input of a gate.
5. In most design situations, the logic gate should consume as little power (and area in an IC design) as needed to meet the speed requirements of the design.

6.3 DYNAMIC RESPONSE OF LOGIC GATES

In today's environment, even the general public is familiar with the seemingly endless increase in logic performance as we are bombarded with marketing of the latest microprocessors in terms of their clock frequencies, 500 MHz, 750 MHz, 1 GHz, and so on. The clock rate of a processor is ultimately set by the dynamic performance of the individual logic circuits. In engineering terms, the time domain performance of a logic family is cast in terms of its average propagation delay, rise time, and fall time as defined in this section.

[2] In some cases, this simple definition can yield a negative value for one of the noise margins.

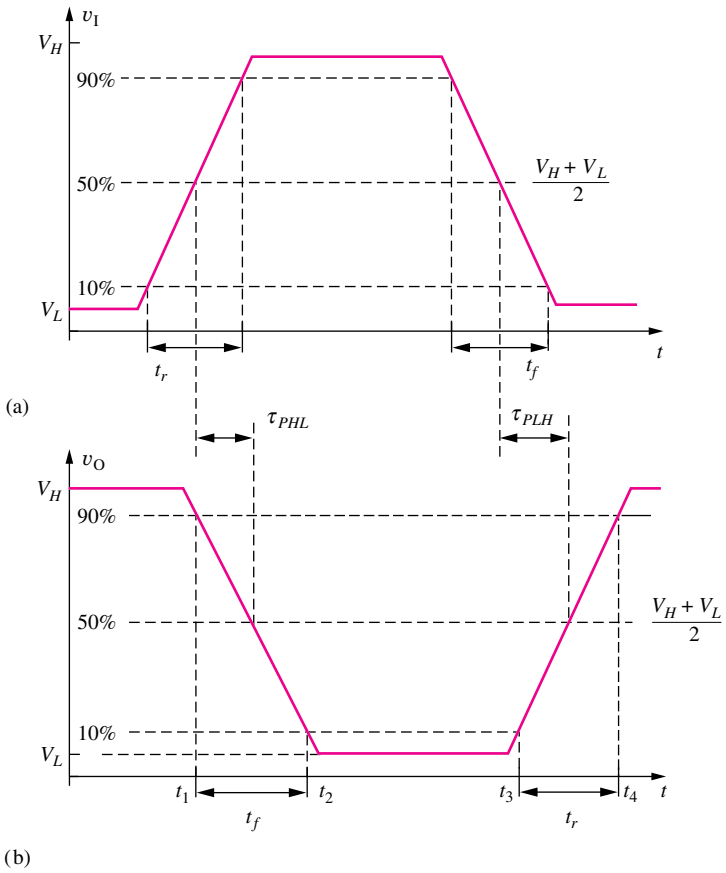


Figure 6.5 Switching waveforms for an *idealized* inverter: (a) input voltage signal, (b) output voltage waveform.

Figure 6.5 shows idealized time domain waveforms for an inverter. The input and output signals are switching between the two static logic levels V_{OL} and V_{OH}. Because of capacitances in the circuits, the waveforms exhibit nonzero rise and fall times, and propagation delays occur between the switching times of the input and output waveforms.

6.3.1 Rise Time and Fall Times

The **rise time** t_r for a given signal is defined as the time required for the signal to make the transition from the **"10 percent" point** to the **"90 percent" point** on the waveform, as indicated in Fig. 6.5. The **fall time** t_f is defined as the time required for the signal to make the transition between the 90 percent point and the 10 percent point on the waveform. The voltages corresponding to the 10 percent and 90 percent points are defined in terms of V_L and V_H and the logic swing ΔV:

$$\begin{aligned} V_{10\%} &= V_L + 0.1\,\Delta V \\ V_{90\%} &= V_L + 0.9\,\Delta V = V_H - 0.1\,\Delta V \end{aligned} \tag{6.3}$$

where $\Delta V = V_H - V_L$. Rise and fall times usually have unequal values; the characteristic shapes of the input and output waveforms also differ.

6.3.2 Propagation Delay

Propagation delay is measured as the difference in time between the input and output signals reaching the **"50 percent" points** in their respective transitions. The 50 percent point is the voltage level corresponding to one-half the total transition between V_H and V_L:

$$V_{50\%} = \frac{V_H + V_L}{2} \tag{6.4}$$

The **propagation delay** on the **high-to-low output transition** is τ_{PHL} and that of the **low-to-high transition** is τ_{PLH}. In the general case, these two delays will not be equal, and the **average propagation delay** τ_P is defined by

$$\tau_P = \frac{\tau_{PLH} + \tau_{PHL}}{2} \tag{6.5}$$

Average propagation delay is one figure of merit that is commonly used to compare the performance of different logic families. In Chapters 6, 7, and 9 we explore the propagation delays for various MOS and bipolar logic circuits.

Exercise: Suppose the waveforms in Fig. 6.5 are those of an ECL gate with $V_L = -2.6$ V and $V_H = -0.6$ V, and $t_1 = 100$ ns, $t_2 = 105$ ns, $t_3 = 150$ ns, and $t_4 = 153$ ns. What are the values of $V_{10\%}$, $V_{90\%}$, $V_{50\%}$, t_r, and t_f?

Answers: -2.4 V; -0.8 V; -1.6 V; 3 ns; 5 ns

6.3.3 Power-Delay Product

The overall performance of a logic family is ultimately determined by how much energy is required to change the state of the logic circuit. The traditional metric for comparing various logic families is the power-delay product, which tells us the amount of energy that is required to perform a basic logic operation.

Figure 6.6 shows the behavior of the average propagation delay of a general logic gate versus the average power supplied to the gate. The power consumed by a gate can be changed by increasing or decreasing the sizes of the transistors and resistors in the gate or by changing the power supply voltage. At low power levels, gate delay is dominated by intergate wiring capacitance, and the delay decreases as power increases. As device size and power are increased further, circuit delay becomes limited by the inherent speed of the electronic switching devices, and the delay becomes independent of power. In bipolar logic technology, the properties of the transistors begin to degrade at even higher power levels, and the delay can actually become worse as power increases further, as indicated in Fig. 6.6.

In the low power region, the propagation delay decreases in direct proportion to the increase in power. This behavior corresponds to a region of constant **power-delay product (PDP),**

$$\text{PDP} = P\tau_P \tag{6.6}$$

in which P is the average power dissipated by the logic gate. The PDP represents the energy (Joules) required to perform a basic logic operation and is another figure of merit widely used to compare logic families.

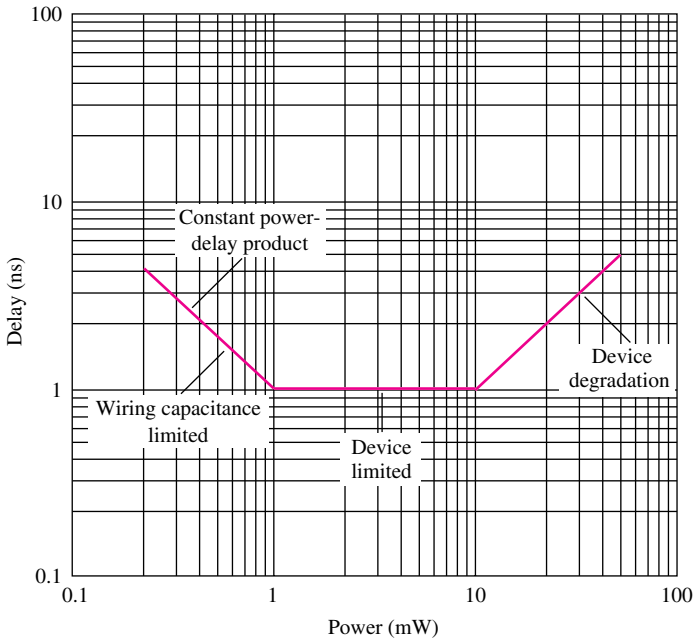


Figure 6.6 Logic gate delay versus power dissipation.

Early logic families had power-delay products of 10 to 100 pJ (1 pJ $= 10^{-12}$ J), whereas many of today's IC logic families now have PDPs in the 10 to 100 fJ range (1 fJ $= 10^{-15}$ J). It has been estimated that the minimum energy required to reliably differentiate two logic states is on the order of $(\ln 2)kT$, which is approximately 4×10^{-20} J at room temperature [4]. Thus even today's best logic families have power-delay products that are many orders of magnitude from the ultimate limit [5].

EXERCISE: (a) What is the power-delay product at low power for the logic gate characterized by Fig. 6.6? (b) What is the PDP at $P = 3$ mW? (c) At 20 mW?

ANSWERS: 1 pJ; 3 pJ; 40 pJ

6.4 REVIEW OF BOOLEAN ALGEBRA

In order to be able to effectively deal with logic system analysis and design, we need a mathematical representation for networks of logic gates. Fortunately, way back in 1849, G. Boole [6] presented a powerful mathematical formulation for dealing with logical thought and reasoning, and the formal algebra we use today to manipulate binary logic expressions is known as **Boolean algebra.** Tables 6.1 to 6.6 and the following discussion summarize Boolean algebra.

Table 6.1 lists the basic logic operations that we need. The logic function at the gate output is represented by variable Z and is a function of logical input variables A and B: $Z = f(A, B)$. To perform general logic operations, a logic family must provide logical inversion (NOT) plus at least one other function of two input variables, such as the OR or AND functions. We will find in Chapter 7 that NMOS logic can easily be used to implement **NOR gates** as well as **NAND gates,** and in Chapter 9 we will see that the basic TTL gate provides a NAND function whereas

TABLE 6.1
Basic Boolean Operations

OPERATION	BOOLEAN REPRESENTATION
NOT	$Z = \overline{A}$
OR	$Z = A + B$
AND	$Z = A \cdot B = AB$
NOR	$Z = \overline{A + B}$
NAND	$Z = \overline{A \cdot B} = \overline{AB}$

TABLE 6.2
NOT (Inverter) Truth Table

A	$Z = \overline{A}$
0	1
1	0

TABLE 6.3
OR Gate Truth Table

A	B	$Z = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

TABLE 6.4
AND Gate Truth Table

A	B	$Z = AB$
0	0	0
0	1	0
1	0	0
1	1	1

OR/NOR logic is provided by the basic ECL gate. Note in Table 6.1 that the NOT function is equivalent to the output of either a single input NOR gate or NAND gate.

Truth tables and logic symbols for the five functions in Table 6.1 appear in Tables 6.2 to 6.6 and Figs. 6.7 to 6.9. The truth table presents the output Z for all possible combinations of the input variables A and B. The inverter, $Z = \overline{A}$, has a single input, and the output represents the logical inversion or complement of the input variable, as indicated by the overbar (Table 6.2; Fig. 6.7).

Tables 6.3 and 6.4 are the truth tables for a two-input **OR gate** and a two-input **AND gate,** respectively, and the corresponding logic symbols appear in Fig. 6.8. The OR operation is indicated by the $+$ symbol; its output Z is a 1 when either one or both of the input variables A or B is a 1. The output is a 0 only if both inputs are 0. The AND operation is indicated by the $\cdot$ symbol, as in $A \cdot B$, or in a more compact form as simply AB, and the output Z is a 1 only if both the input variables A and B are in the 1 state. If either input is 0, then the output is 0. We shall use AB to represent A AND B throughout the rest of this text.

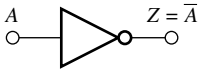


Figure 6.7 Inverter symbol.

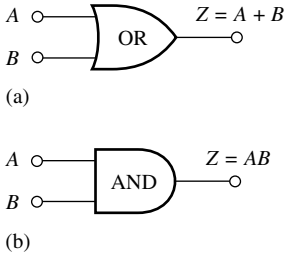


Figure 6.8 (a) OR gate symbol. (b) AND gate symbol.

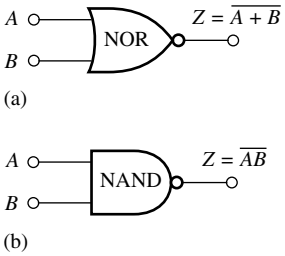


Figure 6.9 (a) NOR gate symbol. (b) NAND gate symbol.

TABLE 6.5
NOR Gate Truth Table

A	B	$Z = \overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0

TABLE 6.6
NAND Gate Truth Table

A	B	$Z = \overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

Tables 6.5 and 6.6 are the truth tables for the two-input NOR gate and the two-input NAND gate, respectively, and the logic symbols appear in Fig. 6.9. These functions represent the complements of the OR and AND operations — that is, the OR or AND operations followed by logical inversion. The NOR operation is represented as $Z = \overline{A + B}$, and its output Z is a 1 only if both inputs are 0. For the NAND operation, $Z = \overline{AB}$, output Z is a 1 except when both the input variables A or B are in the 1 state.

In this chapter and Chapter 8, we will find that a major advantage of MOS logic is its capability to readily form more complex logic functions, particularly logic expressions represented in a complemented **sum-of-products** form:

$$Z = \overline{AB + CD + E} \qquad \text{or} \qquad Z = \overline{ABC + DE} \tag{6.7}$$

The Boolean identities that are shown in Table 6.7 can be very useful in finding simplified logic expressions, such as those expressions in Eq. (6.7). This table includes the identity operations as well as the basic commutative, associative, and distributive laws of Boolean algebra.

TABLE 6.7
Useful Boolean Identities

$A + 0 = A$	$A \cdot 1 = A$	Identity operation
$A + B = B + A$	$AB = BA$	Commutative law
$A + (B + C) = (A + B) + C$	$A(BC) = (AB)C$	Associative law
$A + BC = (A + B)(A + C)$	$A(B + C) = AB + AC$	Distributive law
$A + \overline{A} = 1$	$A \cdot \overline{A} = 0$	Complements
$A + A = A$	$A \cdot A = A$	Idempotency
$A + 1 = 1$	$A \cdot 0 = 0$	Null elements
$\overline{A} + \overline{B} = \overline{AB}$	$\overline{AB} = \overline{A} + \overline{B}$	DeMorgan's theorem

EXAMPLE 6.1 LOGIC EXPRESSION SIMPLIFICATION

Here is an example of the use of Boolean identities to simplify a logic expression.

PROBLEM Use the Boolean relationships in Table 6.7 to show that the expression

$$Z = A\overline{B}C + ABC + \overline{A}BC \qquad \text{can be reduced to} \qquad Z = (A + B)C.$$

SOLUTION **Known Information and Given Data:** Two expressions for Z just given; Boolean identities in Table 6.7

Unknowns: Proof that Z is equivalent to $(A + B)C$

Approach: Apply various identities from Table 6.7 to simplify the formula for Z

Assumptions: None

Analysis:

$$Z = A\overline{B}C + ABC + \overline{A}BC$$

$$Z = A\overline{B}C + ABC + ABC + \overline{A}BC \qquad \text{using } ABC = ABC + ABC$$

$$Z = A(\overline{B} + B)C + (\overline{A} + A)BC \qquad \text{using distributive law}$$

$$Z = A(1)C + (1)BC \qquad \text{using } (\overline{B} + B) = (B + \overline{B}) = 1$$

$$Z = AC + BC \qquad \text{since } A(1)C = AC(1) = AC$$

$$Z = (A + B)C \qquad \text{using distributive law}$$

Check of Results: We have reached the desired answer. A double check indicates the sequence of steps appears valid.

EXERCISE: Simplify the logic expression $Z = (A + B)(B + C)$

ANSWER: $Z = B + AC$

6.5 DIODE LOGIC AND DTL

Diode logic is one of the simplest circuit techniques that can be used to implement the AND and OR functions. Although of somewhat limited utility, diode logic provides a simple introduction to logic circuit implementation and can be used in circuit design to logically combine several input signals.

6.5.1 DIODE OR GATE

Figure 6.10 is the circuit diagram of a simple diode OR gate along with circuit voltages for the case $A = 1$ or 5 V and $B = 0$ or 0 V. In Fig. 6.10(b), diode D_1 is conducting, diode D_2 is reverse-biased, and the output voltage is one diode voltage drop below the 5 V input at A. Using

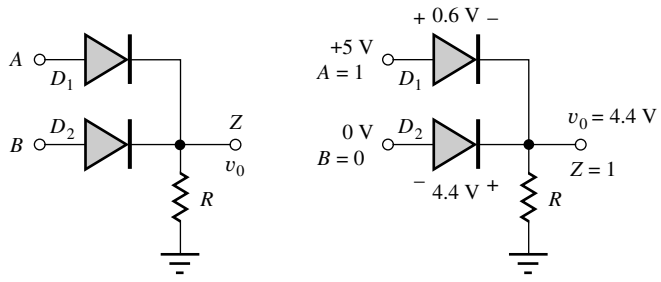


Figure 6.10 (a) Diode OR gate. (b) OR gate with $A = 1$ and $B = 0$.

the constant-voltage-drop model from Chapter 3 with $V_{on} = 0.6$ V, $v_0 = 5$ V $- 0.6$ V $= 4.4$ V and $Z = 1$. Although the output voltage is not equal to the full 5-V input level, 4.4 V is usually sufficiently large to be interpreted as a logical 1. If at least one of the inputs in the circuit in Fig. 6.10 is at +5 V, then the output of this gate will be at 4.4 V. If both inputs are at 0 V, then D_1 and D_2 will both be nonconducting and $v_0 = 0$. Thus, the diode circuit in Fig. 6.10 is a basic form of OR logic.

6.5.2 Diode AND Gate

By reversing the diodes and power supply, as in Fig. 6.11, the circuit becomes an AND gate. In Fig. 6.11(b), we again look at the circuit for the case $A = 1$ (5 V) and $B = 0$ (0 V). Diode D_1 is now reverse-biased, diode D_2 is conducting, and the output voltage is one diode voltage drop above ground potential:

$$v_0 = (0 + 0.6) \text{ V} = 0.6 \text{ V} \qquad \text{and} \qquad Z = 0$$

Although the output voltage is not equal to 0 V, the 0.6-V level is sufficiently low to be interpreted as a logical 0. If either one or both of the inputs is at 0 V, then the output of the gate is 0.6 V. Only if both inputs are at +5 V will the output also be at +5 V, corresponding to $Z = 1$. Thus, the circuit in Fig. 6.11 functions as a basic AND gate.

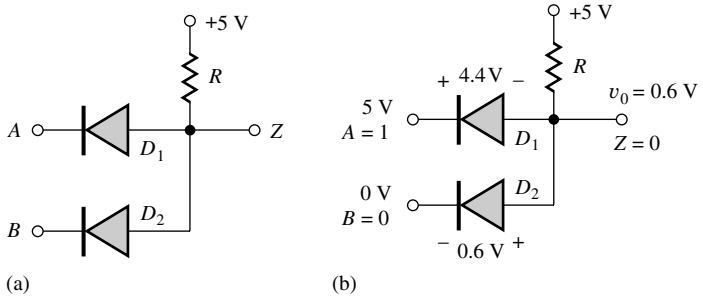


Figure 6.11 (a) Diode AND gate. (b) AND gate with $A = 1$, $B = 0$, and $Z = 0$.

Although the diode OR and AND gates provide simple implementations of their respective logic function, they both suffer from the same problem. The gates do not satisfy design goal 3 discussed in Sec. 6.2 because the logic levels are not regenerated at the output of the gate. When several similar gates are connected in series, the output level is degraded one diode drop by each gate in the chain. If too many diode logic gates are cascaded, then the output voltage no longer represents the proper binary state. However, there are often cases where the circuit designer would like to form the AND or OR combination of several logical variables in a simple control circuit, and diode logic will suffice.

6.5.3 A Diode-Transistor Logic (DTL) Gate

The level-restoration problem associated with diode logic can be solved by adding a diode and transistor to form the **diode-transistor logic (DTL)** gate shown schematically in Fig. 6.12. We will analyze bipolar logic gates in detail in Chapter 9; here is a brief overview of the operation of this gate.

The situation in Fig. 6.13(a) corresponds to the case in which both inputs are in the logical 1 state, $V_H = V_+ = 3.3$ V. In this particular circuit, diodes D_1 and D_2 are both off, whereas D_3 and Q_1 are on. Node 1 is at 1.3 V:

$$V_1 = V_{D3} + V_{BE} = 0.6 \text{ V} + 0.7 \text{ V} = 1.3 \text{ V}$$

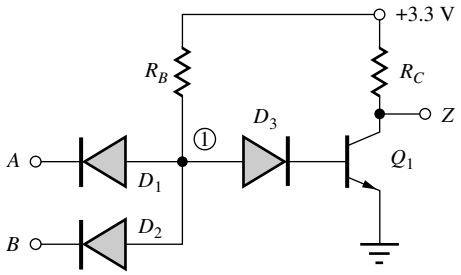


Figure 6.12 A two-input diode-transistor logic (DTL) NAND gate.

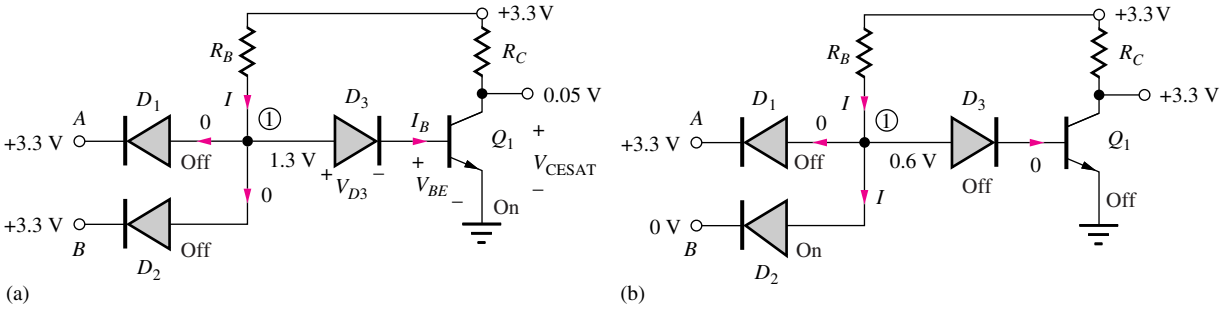


Figure 6.13 A diode-transistor NAND gate: (a) both inputs high, (b) one input low.

The current I through resistor R_B and diode D_3 becomes the base current I_B of transistor Q_1. The value of I_B is designed to cause Q_1 to saturate so that $v_O = V_{CESAT}$ (for example, 0.05 to 0.1 V).

In Fig. 6.13(b), input B is now at 0 V, corresponding to a logical 0. Diode D_2 is conducting, holding node 1 at 0.6 V. Now diode D_3 and transistor Q_1 must both be off, because the voltage at node 1 is now less than the two diode voltage drops required to turn on both D_3 and Q_1. The base current of Q_1 is now zero; Q_1 will be off with $I_C = 0$, and the output voltage will be at +3.3 V, corresponding to a logical 1. A similar situation holds for the circuit if both inputs are low. The truth table for this gate is identical to Table 6.6. The DTL circuit represents a two-input NAND gate with $Z = \overline{AB}$.

EXERCISE: What is the base current in transistor Q_1 in Fig. 6.13(a) if $R_B = 100$ kΩ?

ANSWER: 20 μA

6.6 NMOS LOGIC DESIGN

The rest of Chapter 6 focuses on understanding the design of MOS logic gates that use only n-channel MOS transistors (NMOS logic) or p-channel MOS transistors (PMOS logic). Study of these circuits employing **single-channel technology** provides a background for understanding many important logic circuit concepts as well as the improvements gained by going to CMOS circuitry, which is the topic for Chapter 7. The discussion begins by investigating the design of the MOS inverter in order to gain an understanding of its voltage transfer characteristic and noise margins. Inverters with four different load configurations are considered: the resistor load,

saturated load, linear load, and depletion-mode load circuits. NOR, NAND, and more complex logic gates can be easily designed as simple extensions of the reference inverter designs. Later, the rise time, fall time, and propagation delays of the gates are analyzed.

The drain current of the MOS device depends on its gate-source voltage v_{GS}, drain-source voltage v_{DS}, and source-bulk voltage v_{SB}, and on the device parameters, which include the transconductance parameter K_n', threshold voltage V_{TN}, and width-to-length or ***W/L* ratio.** The power supply voltage constrains the range of v_{GS} and v_{DS}, and the technology sets the values of K_n' and V_{TN}. Thus, the circuit designer's job is to choose the circuit topology and the W/L ratios of the MOS transistors to achieve the desired logic function.

In most logic design situations, the power supply voltage is predetermined by either technology reliability constraints or system-level criteria. For example, as mentioned in Sec. 6.1, V_{DD}[3] = 5.0 V has been the standard power supply for logic for many years. However, a new 3.3-V power supply level is now gaining widespread use as well. In addition, many portable low-power systems, such as cell phones and PDAs, must operate from battery voltages as low as 1.0 to 1.5 V.

We begin our study of MOS logic circuit design by considering the detailed design of the NMOS inverter with the resistor load that was introduced in Chapter 5. Although we will seldom use this exact circuit, it provides a good basis for understanding operation of the basic logic gate. In integrated logic circuits, the load resistor occupies too much silicon area, and is replaced by a second NMOS transistor. This "load device" can be connected in three different configurations called the saturated load, linear load, and depletion-mode load circuits. We will explore the design of the NMOS load configurations in detail in this and Secs. 6.7 through 6.10.

6.6.1 NMOS Inverter with Resistive Load

Complex digital systems can consist of millions of logic gates, and it is helpful to remember that each individual logic gate is generally interconnected in a larger network. The output of one logic gate drives the input of another logic gate, as shown schematically by the four inverters in Fig. 6.14. Thus, a gate has $v_O = V_H$ when an input voltage $v_I = V_L$ is applied to its input, and vice versa. For MOS design, we first need to find V_H and then apply it as an input to the gate in order to determine V_L.

The basic inverter circuit shown in Fig. 6.15 consists of an NMOS switching device M_S designed to force v_O to V_L and a **resistor load** element to "pull" the output up toward the power supply V_{DD}. The NMOS transistor is designed to switch between the triode region for $v_I = V_H$ and the cutoff (nonconducting) state for $v_I = V_L$. The circuit designer must choose the values of the load resistor R and the W/L ratio of **switching transistor** M_S so the inverter meets a set of design specifications. In this case, these two design variables permit us to choose the V_L level and set the total power dissipation of the logic gate.

Let us explore the inverter operation by considering the requirements for the design of such a logic gate. Writing the equation for the output voltage, we find

$$v_O = v_{DS} = V_{DD} - i_D R \tag{6.8}$$

When the input voltage is at a low state, $v_I = V_L$, M_S should be cut off, with $i_D = 0$, so that

$$v_O = V_{DD} = V_H \tag{6.9}$$

Thus, in this particular logic circuit, the value of V_H is set by the power supply voltage $V_{DD} = 5$ V.

[3] V_{DD} and V_{SS} have traditionally been used to denote the positive and negative power supply voltages in MOS circuits.

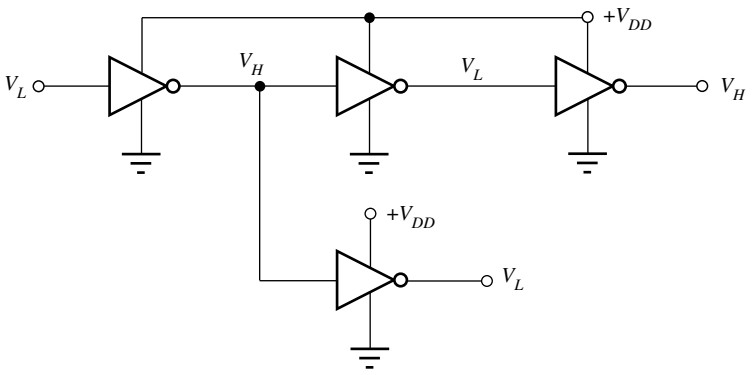


Figure 6.14 A network of inverters.

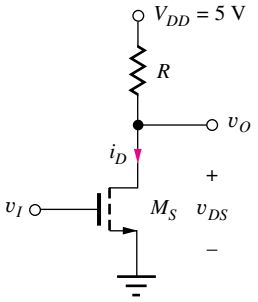


Figure 6.15 NMOS inverter with resistive load.

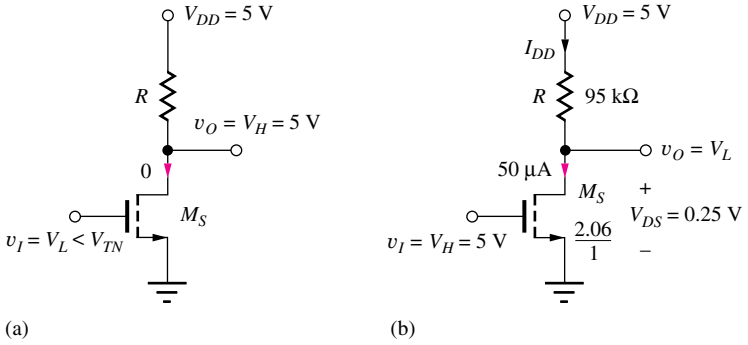


Figure 6.16 Inverters in the (a) $v_I = V_L (0)$ and (b) $v_I = V_H$ (1) logic states.

To ensure that transistor M_S is cut off when the input is equal to V_L, as in Fig. 6.16(a), the gate-source voltage of M_S ($v_{GS} = V_L$) must be less than its threshold voltage V_{TN}. For $V_{TN} = 1$ V, a normal design point would be for V_L to be in the range of 25 to 50 percent of V_{TN} or 0.25 to 0.50 V to ensure adequate noise margins. Let us assume a design value of $V_L = 0.25$ V.

DESIGN NOTE

DESIGN OF V_L

To ensure that switching transistor M_S is cut off when the input is in the low logic state, V_L is designed to be 25 to 50 percent of the threshold voltage of switch M_S. This choice also provides a reasonable value for noise margin NM_L.

6.6.2 Design of the W/L Ratio of M_S

The value of W/L required to set $V_L = 0.25$ V can be calculated if we know the parameters of the MOS device. For now, the values $V_{TN} = 1$ V and $K_n' = 25 \times 10^{-6}$ A/V^2 will be used. In addition, we need to know a value for the desired operating current of the inverter. The current is determined by the permissible power dissipation of the NMOS gate when $v_O = V_L$. Using $P = 0.25$ mW (see

Probs. 6.44 and 6.45),[4] the current in the gate can be found from $P = V_{DD} \times I_{DD}$. For our circuit,

$$0.25 \times 10^{-3} = 5 \times I_{DD} \qquad \text{or} \qquad I_{DD} = 50\ \mu\text{A} = i_D$$

Now we can determine the value for the W/L ratio of the NMOS switching device from the MOS drain current expression using the circuit conditions in Fig. 6.16(b). In this case, the input is set equal to $V_H = 5$ V, and the output of the inverter should then be at V_L. The expression for the drain current in the triode region of the device is used because $v_{GS} - V_{TN} = 5\text{ V} - 1\text{ V} = 4$ V, and $v_{DS} = V_L = 0.25$ V, yielding $v_{DS} < v_{GS} - V_{TN}$.

$$i_D = K_n' \left(\frac{W}{L}\right)_S (v_{GS} - V_{TN} - 0.5v_{DS})\, v_{DS} \tag{6.10}$$

or

$$5 \times 10^{-5}\text{ A} = \left(25 \times 10^{-6} \frac{\text{A}}{\text{V}^2}\right) \left(\frac{W}{L}\right)_S (5\text{ V} - 1\text{ V} - 0.125\text{ V})(0.25\text{ V})$$

Solving Eq. (6.10) for $(W/L)_S$ gives $(W/L)_S = 2.06/1$.

6.6.3 Load Resistor Design

The value of the load resistor R is chosen to limit the current when $v_O = V_L$ and is found from

$$R = \frac{V_{DD} - V_L}{i_D} = \frac{(5 - 0.25)\text{ V}}{5 \times 10^{-5}\text{ A}} = 95\text{ k}\Omega \tag{6.11}$$

These design values are shown in the circuit in Fig. 6.16(b).

Exercise: **Redesign the logic gate in Fig. 6.16 to operate at a power of 0.5 mW while maintaining $V_L = 0.25$ V.**

Answer: **$(W/L)_S = 4.12/1$; $R = 47.5\ \text{k}\Omega$**

6.6.4 Load-Line Visualization

An important way to visualize the operation of the inverter is to draw the load line on the MOS transistor output characteristics as in Fig. 6.17. Equation (6.8), repeated here, represents the equation for the load line:

$$v_{DS} = V_{DD} - i_D R$$

When the transistor is cut off, $i_D = 0$ and $v_{DS} = V_{DD} = 5$ V, and when the transistor is on, the MOSFET is operating in the triode region, with $v_{GS} = V_H = 5$ V and $v_{DS} = v_O = V_L = 0.25$ V. The MOSFET switches between the two operating points on the load line, as indicated by the circles in Fig. 6.17. At the right-hand end of the load line, the MOSFET is cut off. At the Q-point near the left end of the load line, the MOSFET represents a relatively low resistance, and the current is determined primarily by the load resistance. (Note how the Q-point is nearly independent of v_{GS}.)

[4] It would be worth exploring these problems before continuing.

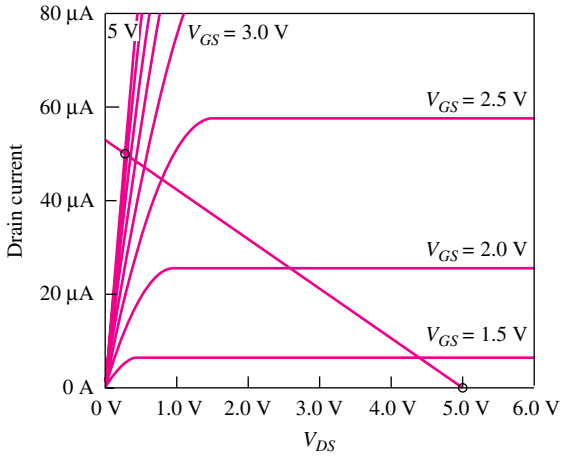


Figure 6.17 MOSFET output characteristics and load line.

DESIGN EXAMPLE 6.2 DESIGN OF AN INVERTER WITH RESISTIVE LOAD

Design a resistively loaded NMOS inverter to operate from a 3.3-V power supply.

PROBLEM Design an inverter with a resistive load for $V_{DD} = 3.3$ V and $P = 0.1$ mW with $V_L = 0.2$ V. Assume $K_n' = 60\ \mu\text{A/V}^2$ and $V_{TN} = 0.75$ V.

SOLUTION **Known Information and Given Data:** Circuit topology in Fig. 6.15; $V_{DD} = 3.3$ V, $P = 0.1$ mW, $V_L = 0.2$ V, $K_n' = 60\ \mu\text{A/V}^2$, and $V_{TN} = 0.75$ V

Unknowns: Value of load resistor R; W/L ratio of switching transistor M_S

Approach: Use the power dissipation specification to find the current I_{DD} for $v_O = V_L$. Use V_{DD}, V_L, and I_{DD} to calculate R. Determine V_H. Use V_H, V_L, and I_{DD} to find $(W/L)_S$.

Assumptions: M_S is off for $v_I = V_L$; M_S is in the triode region for $v_O = V_L$.

Analysis: Using the power specification with the inverter circuit in Fig. 6.15, we have

$$I_{DD} = \frac{P}{V_{DD}} = \frac{10^{-4}\ \text{W}}{3.3\ \text{V}} = 30.3\ \mu\text{A}$$

$$R = \frac{V_{DD} - V_L}{I_{DD}} = \frac{3.3 - 0.2}{30.3}\frac{\text{V}}{\mu\text{A}} = 102\ \text{k}\Omega$$

For $v_I = V_L = 0.2$ V, the MOSFET will be off since 0.2 V is less than the threshold voltage, and the output high level will be $V_H = V_{DD} = 3.3$ V. The triode region expression for the MOSFET drain current with $v_{GS} = v_I = V_H$ and $v_{DS} = v_O = V_L$ is

$$I_D = K_n'\left(\frac{W}{L}\right)_S\left(V_H - V_{TN} - \frac{V_L}{2}\right)V_L$$

Equating this expression to the drain current yields

$$30.3\ \mu\text{A} = (60 \times 10^{-6})\left(\frac{W}{L}\right)_S \left(3.3 - 0.75 - \frac{0.2}{2}\right) 0.2 \rightarrow \left(\frac{W}{L}\right)_S = \frac{1.03}{1}$$

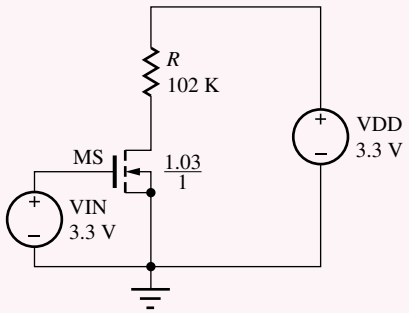
Thus our completed design values are $R = 102\ \text{k}\Omega$ and $(W/L)_S = 1.03/1$.

Check of Results: We should check the triode region assumption for the MOSFET for $v_O = V_L$: $V_{GS} - V_{TN} = 3.3 - 0.75 = 2.55$ V, which is indeed greater than $V_{DS} = 0.2$ V. Let us also double check the value of W/L by using it to calculate the drain current:

$$I_D = (60 \times 10^{-6})\left(\frac{1.03}{1}\right)\left(3.3 - 0.75 - \frac{0.2}{2}\right) 0.2 = 30.3\ \mu\text{A} \quad \checkmark$$

Discussion: This new design for a reduced voltage and reduced power requires a larger value of load resistor to limit the current, but a smaller device to conduct the reduced level of current.

Computer-Aided Analysis: Let us verify our design values with SPICE. The circuit drawn with a schematic capture tool is given below. The NMOS transistor uses the LEVEL = 1 model with KP = 6.0E-5, VTO = 1, W = 1.03U, and L = 1U. The Q-point of the transistor is (30.4 μA, 0.201 V), which agrees with the design specifications.



EXERCISE: (a) Redesign the inverter in Ex. 6.2 to have $V_L = 0.1$ V with $R = 102\ \text{k}\Omega$. (b) Verify your design with SPICE.

ANSWER: $(W/L)_S = 2.09/1$

6.6.5 On-Resistance of the Switching Device

When the logic gate output is in the low state, the output voltage can also be calculated from a resistive voltage divider formed by the load resistor R and the **on-resistance** R_{on} of the MOSFET, as in Fig. 6.18.

$$V_L = V_{DD}\frac{R_{\text{on}}}{R_{\text{on}} + R} = V_{DD}\frac{1}{1 + \dfrac{R}{R_{\text{on}}}} \tag{6.12}$$

where

$$R_{\text{on}} = \frac{v_{DS}}{i_D} = \frac{1}{K_n'\dfrac{W}{L}\left(v_{GS} - V_{TN} - \dfrac{v_{DS}}{2}\right)} \tag{6.13}$$

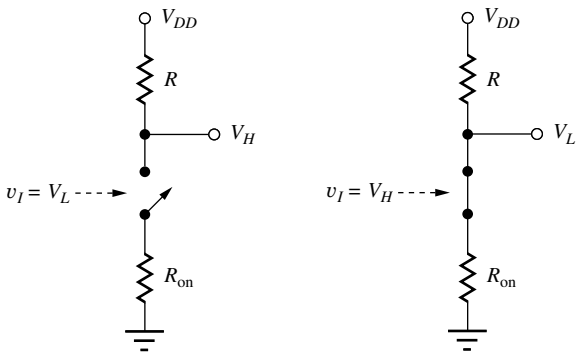


Figure 6.18 Simplified representation of an inverter: (a) the off or nonconducting state, (b) the on or conducting state.

R_{on} must be much smaller than R in order for V_L to be small. It is important to recognize that R_{on} represents a nonlinear resistor because the value of R_{on} is dependent on v_{DS}, the voltage across the resistor terminals. All the NMOS gates that we study in this chapter demonstrate **"ratioed" logic** — that is, designs in which the on-resistance of the switching transistor must be much smaller than that of the load resistor in order to achieve a small value of V_L ($R_{on} \ll R$).

EXAMPLE 6.3 ON-RESISTANCE CALCULATION

Find the on-resistance for the MOSFET in the completed inverter design in Fig. 6.16(b).

PROBLEM What is the value of the on-resistance for the NMOS FET in Fig. 6.16 when the output voltage is at V_L?

SOLUTION **Known Information and Given Data:** $K_n' = 25\ \mu\text{A/V}^2$, $V_{TN} = 1$ V, $W/L = 2.06/1$, $V_{DS} = V_L = 0.25$ V

Unknowns: On-resistance of the switching transistor

Approach: Use the known values to evaluate Eq. (6.13).

Assumptions: The transistor is in the triode region of operation.

Analysis: R_{on} can be found using Eq. (6.13).

$$R_{on} = \frac{1}{\left(25 \times 10^{-6}\dfrac{\text{A}}{\text{V}^2}\right)\left(\dfrac{2.06}{1}\right)\left(5 - 1 - \dfrac{0.25}{2}\right)\text{V}} = 5.0\ \text{k}\Omega$$

Check of Results: We can check this value by using it to calculate V_L:

$$V_L = V_{DD}\frac{R_{on}}{R_{on} + R} = 5\ \text{V}\frac{5\ \text{k}\Omega}{5\ \text{k}\Omega + 95\ \text{k}\Omega} = 0.25\ \text{V}$$

$R_{on} = 5\ \text{k}\Omega$ does indeed give the correct value of V_L. Note that $R_{on} \ll R$. Checking the triode region assumption: $V_{GS} - V_{TN} = 5 - 1 = 4$ V and $V_{DS} = V_L = 0.25$ V. ✔

EXERCISE: What value of R_{on} is indeed to set $V_L = 0.20$ V? What is the new value of W/L needed for the MOSFET to achieve this value of R_{on}?

ANSWERS: 3.96 kΩ; 2.59/1

EXERCISE: What is the value of R_{on} for the MOSFET in Ex. 6.2? Use R_{on} to find V_L.

ANSWERS: 6.61 kΩ; 0.201 V

6.6.6 NOISE MARGIN ANALYSIS

Figure 6.19 is a SPICE simulation of the voltage transfer function for the completed inverter design from Fig. 6.16. Now we are in a position to find the values of V_{IL}, V_{OL}, V_{IH}, and V_{OH} that correspond to the points at which the slope of the voltage transfer characteristic for the inverter is equal to -1, as defined in Sec. 6.2. Our analysis begins with the expression for the load line, repeated here from Eq. (6.8):

$$v_O = V_{DD} - i_D R \tag{6.14}$$

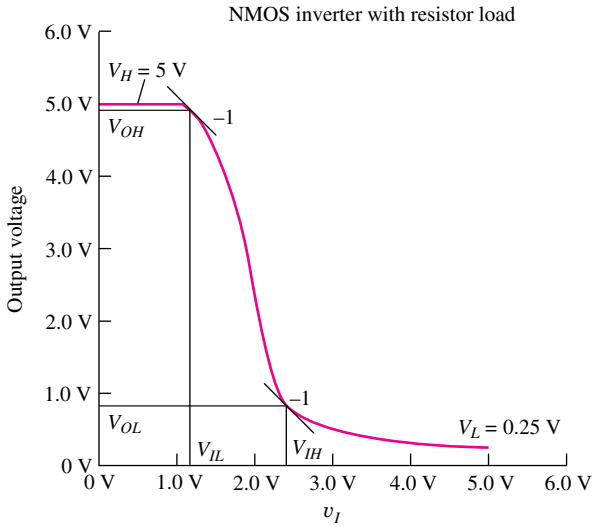


Figure 6.19 Simulated voltage transfer characteristic of an NMOS logic gate with resistive load.

6.6.7 CALCULATION OF V_{IL} AND V_{OH}

Referring back to Fig. 6.15 with $v_I = V_{IL}$, v_{GS} $(= v_I)$ is small and v_{DS} $(= v_O)$ is large, so we expect the MOSFET to be operating in saturation, with drain current given by

$$i_D = (K_n/2)(v_{GS} - V_{TN})^2 \qquad \text{where } K_n = K_n'(W/L) \text{ and } v_{GS} = v_I$$

Substituting this expression for i_D in load-line Eq. (6.14),

$$v_O = V_{DD} - \frac{K_n}{2}(v_I - V_{TN})^2 R \tag{6.15}$$

and taking the derivative of v_O with respect to v_I results in

$$\frac{dv_O}{dv_I} = -K_n(v_I - V_{TN})R \tag{6.16}$$

Setting this derivative equal to -1 for $v_I = V_{IL}$ yields

$$V_{IL} = V_{TN} + \frac{1}{K_n R} \qquad \text{with} \qquad V_{OH} = V_{DD} - \frac{1}{2K_n R} \tag{6.17}$$

We see that the value of V_{IL} is slightly greater than V_{TN}, since the input must exceed V_{TN} for M_S to begin conduction, and V_{OH} is slightly less than V_{DD}. The $1/K_n R$ terms represent the ratio of the transistor's transconductance parameter to the value of the load resistor. As K_n increases for a given value of R, V_{IL} decreases and V_{OH} increases.

EXERCISE: Show that $(1/K_n R)$ has the units of voltage.

6.6.8 CALCULATION OF V_{IH} AND V_{OL}

For $v_I = V_{IH}$, v_{GS} is large and v_{DS} is small, so we now expect the MOSFET to be operating in the triode region with drain current given by $i_D = K_n[v_{GS} - V_{TN} - (v_{DS}/2)]v_{DS}$. Substituting this expression for i_D into Eq. (6.14) and realizing that $v_O = v_{DS}$ yields

$$v_O = V_{DD} - K_n R\left(v_I - V_{TN} - \frac{v_O}{2}\right) v_O$$

or

$$\frac{v_O^2}{2} - v_O\left[v_I - V_{TN} + \frac{1}{K_n R}\right] + \frac{V_{DD}}{K_n R} = 0 \tag{6.18}$$

Solving for v_O and then setting $dv_O/dv_I = -1$ for $v_I = V_{IH}$ yields

$$V_{IH} = V_{TN} - \frac{1}{K_n R} + 1.63\sqrt{\frac{V_{DD}}{K_n R}} \qquad \text{with} \qquad V_{OL} = \sqrt{\frac{2V_{DD}}{3K_n R}} \tag{6.19}$$

In this case, we find that the values of V_{OL} and V_{IH} depend on the ratio $V_{DD}/K_n R$.

EXAMPLE 6.4 NOISE MARGIN CALCULATION FOR THE RESISTIVE LOAD INVERTER

Find the noise margins associated with the inverter design in Fig. 6.16(b).

PROBLEM Calculate the noise margins for the inverter in Fig. 6.16(b).

SOLUTION **Known Information and Given Data:** The NMOS inverter circuit with resistor load in Fig. 6.15 with $R = 95\ \text{k}\Omega$, $(W/L)_S = 2.06/1$, $K_n' = 25\ \mu\text{A/V}^2$, and $V_{TN} = 1\ \text{V}$

Unknowns: The values of V_{IL}, V_{OH}, V_{IH}, V_{OL}, NM_L, and NM_H

Approach: Use the given data to evaluate Eqs. (6.17) and (6.18). Use the results to find the noise margins: $\text{NM}_H = V_{OH} - V_{IH}$ and $\text{NM}_L = V_{IL} - V_{OL}$.

Assumptions: Equation (6.17) assumes saturation region operation; Eq. (6.18) assumes triode region operation.

Analysis: For the inverter design in Fig. 6.16(b),

$$V_{TN} = 1\ \text{V} \qquad K_n'\frac{W}{L} = 25\frac{2.06}{1}\frac{\mu\text{A}}{\text{V}^2} = 51.5\frac{\mu\text{A}}{\text{V}^2} \qquad R = 95\ \text{k}\Omega$$

Evaluating Eq. (6.17),

$$V_{IL} = 1 + \frac{1}{(51.5\ \mu\text{A})(95\ \text{k}\Omega)} = 1.20\ \text{V} \quad \text{and} \quad V_{OH} = 5 - \frac{1}{2(51.5\ \mu\text{A})(95\ \text{k}\Omega)} = 4.90\ \text{V}$$

and Eq. (6.18),

$$V_{IH} = 1 - \frac{1}{(51.5\ \mu\text{A})(95\ \text{k}\Omega)} + 1.63\sqrt{\frac{5}{(51.5\ \mu\text{A})(95\ \text{k}\Omega)}} = 2.44\ \text{V}$$

$$V_{OL} = \sqrt{\frac{2(5)}{3(51.5\ \mu\text{A})(95\ \text{k}\Omega)}} = 0.83\ \text{V}$$

The noise margins are found to be

$$\text{NM}_H = 4.90 - 2.44 = 2.46\ \text{V} \qquad \text{and} \qquad \text{NM}_L = 1.20 - 0.83 = 0.37\ \text{V}$$

Check of Results: The values of V_{IL}, V_{OH}, V_{IH}, and V_{OL} all agree well with the simulation results in Fig. 6.19. Equation (6.17) is based on the assumption of saturation region operation. We should check to see if this assumption is consistent with the results in Eq. (6.17): $v_{DS} = 4.90$ and $v_{GS} - V_{TN} = 1.2 - 1.0 = 0.2$. Because $v_{DS} > (v_{GS} - V_{TN})$, our assumption was correct. Similarly, Eq. (6.18) is based on the assumption of triode region operation. Checking this assumption, we have $v_{DS} = 0.83$ and $v_{GS} - V_{TN} = 2.44 - 1.0 = 1.4$. Since $v_{DS} < (v_{GS} - V_{TN})$, our assumption was correct.

Discussion: Our analysis indicates that a long chain of inverters can tolerate electrical noise and process variations equivalent to 0.37 V in the low-input state and more than 2.4 V in the high state. Note that it is common for the values of the two noise margins to be substantially different, as illustrated here.

EXERCISE: (a) Find the noise margins for the inverter in Ex. 6.2. (b) Verify your results with SPICE.

ANSWERS: $\text{NM}_L = 0.32$ V; $\text{NM}_H = 1.45$ V ($V_{IL} = 0.090$ V, $V_{OH} = 3.22$ V, $V_{IH} = 1.77$ V, $V_{OL} = 0.591$ V)

As mentioned earlier, V_{IL}, V_{OL}, V_{IH}, and V_{OH}, as specified by a manufacturer, actually represent guaranteed specifications for a given logic family and take into account the full range of variations in technology parameters, temperature, power supply, loading conditions, and so on. In Ex. 6.4, we have computed only V_{IL}, V_{OL}, V_{IH}, and V_{OH} and the noise margins under nominal conditions at room temperature.

6.6.9 Load Resistor Problems

The NMOS inverter with resistive load has been used to introduce the concepts associated with static logic gate design. Although a simple discrete component logic gate could be built using this circuit, IC realizations do not use resistive loads because the resistor would take up far too much area.

To explore the load resistor problem further, consider the rectangular block of semiconductor material in Fig. 6.20 with a resistance given by

$$R = \frac{\rho L}{tW} \tag{6.20}$$

where $\rho =$ resistivity

$L, W, t =$ length, width, thickness of resistor, respectively

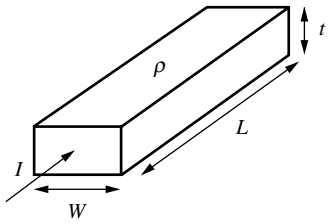


Figure 6.20 Geometry for a simple rectangular resistor.

In an integrated circuit, a resistor might typically be fabricated with a thickness of 1 μm in a silicon region with a resistivity of 0.001 Ω · cm. For these parameters, the 95-kΩ load resistor in the previous section would require the ratio of L/W to be

$$\frac{L}{W} = \frac{Rt}{\rho} = \frac{(9.5 \times 10^4\ \Omega)(1 \times 10^{-4}\ \text{cm})}{0.001\ \Omega \cdot \text{cm}} = \frac{9500}{1}$$

If the resistor width W were made a minimum line width of 1 μm, which we will call the **minimum feature size *F*,** then the length L would be 9500 μm, and the area would be 9500 μm^2.

For the switching device M_S, W/L was found to be 2.06/1. If the device channel length is made equal to the minimum feature size of 1 μm, then the gate area of the NMOS device is only 2.06 μm^2. Thus, the load resistor would consume more than 4000 times the area of the switching transistor M_S. This is simply not an acceptable utilization of area in IC design. The solution to this problem is to replace the load resistor with a transistor.

6.6.10 Transistor Alternatives to the Load Resistor

The two-terminal resistor is replaced with a three-terminal MOSFET, and four possibilities are shown in Fig. 6.21. One possibility is to connect the gate to the source, as in Fig. 6.21(a). However, for this case $v_{GS} = 0$, and MOSFET M_L will be nonconducting, assuming it is an enhancement-mode device with $V_{TN} > 0$. A similar problem exists if the gate is grounded, as in Fig. 6.21(b).

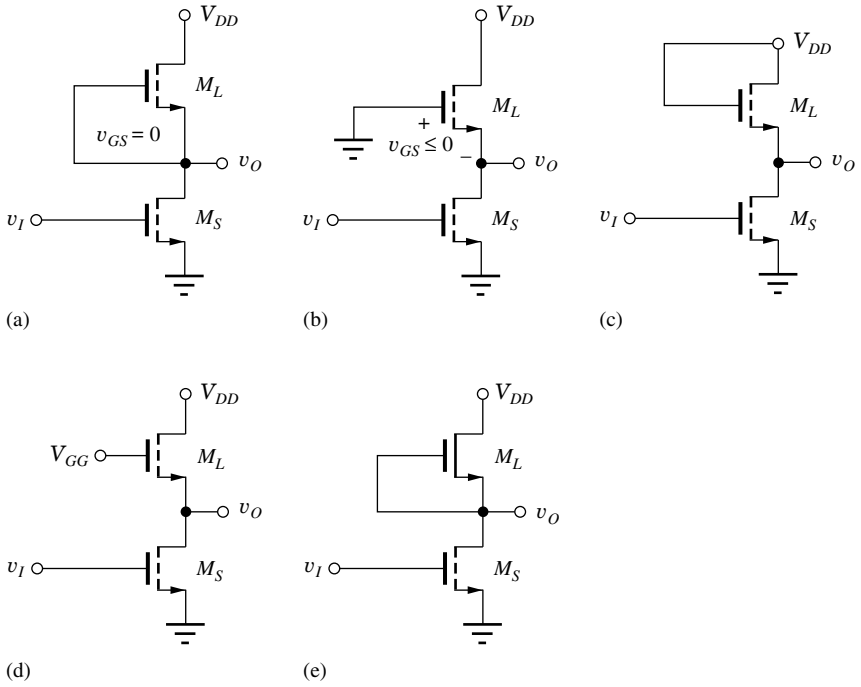


Figure 6.21 NMOS inverter load device options: (a) NMOS inverter with gate of the load device connected to its source, (b) NMOS inverter with gate of the load device grounded, (c) saturated load inverter, (d) linear load inverter, and (e) Depletion load inverter. Note that (a) and (b) are not useful.

Here again, the connection forces $v_{GS} \leq 0$, and the load device is turned off. Neither of these two connections work because an enhancement-mode load device can never conduct current under these conditions.

A workable choice is to connect the gate to the drain, as in Fig. 6.21(c). Here $v_{DS} = v_{GS}$, and the load device will operate in the saturation region because $v_{GS} - V_{TN} = v_{DS} - V_{TN} \leq v_{DS}$ for $V_{TN} \geq 0$. Because the connection forces the **load transistor** to always operate in the saturation region, we refer to this inverter as the **saturated load inverter.** Another solution, called the **linear load inverter,** is shown in Fig. 6.21(d). In this circuit, the gate of the load device is biased by a second voltage that maintains M_L in the triode (linear) region.

The circuit configuration in Fig. 6.21(a) can be made to work if load transistor M_L is converted to a depletion-mode device (i.e., $V_{TN} < 0$), as redrawn in Fig. 6.21(e). This form of NMOS logic provides that highest performance at the cost of additional fabrication process, because the threshold of M_L must be modified to convert it from an enhancement-mode transistor to a depletion-mode device.

Saturated load logic played an important role in the history of electronic circuits. This form of logic was used in the design of the early microprocessors, first in PMOS and later in NMOS technology, and this logic family provides a basic foundation for understanding many of the issues related to MOS VLSI design. Thus, we explore its design in Sec. 6.7.

6.7 STATIC DESIGN OF THE NMOS SATURATED LOAD INVERTER

Figure 6.22(a) shows the circuit diagram for the saturated load inverter, and Fig. 6.22(b) shows the cross section of the inverter in integrated circuit form. Here we see a very important aspect of the structure. The substrate is common to both transistors; thus, the substrate voltage must be the

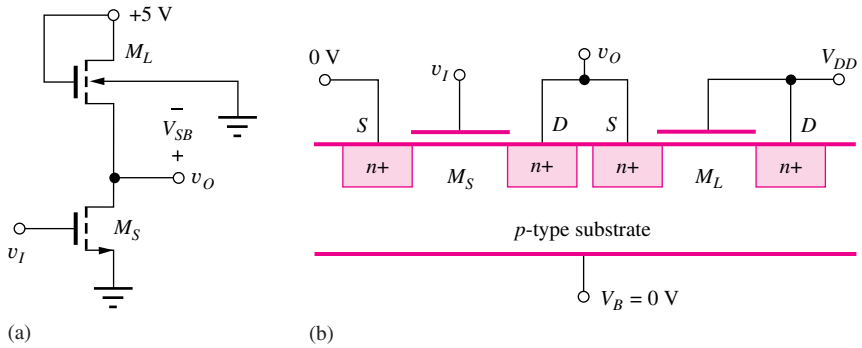


Figure 6.22 (a) Saturated load inverter. (b) Cross section of two integrated MOSFETs forming an inverter.

same for both M_S and M_L in the inverter, and the substrate terminal of M_L cannot be connected to its source as originally indicated in Fig. 6.21(c). This extra substrate terminal is most commonly connected to ground (0 V) (although voltages of -5 V and -8 V have been used in the past). For a substrate voltage of 0 V, v_{SB} for the switching device is always zero, but v_{SB} for the load device M_L changes as v_O changes. In fact, $v_{SB} = v_O$, as indicated in Fig. 6.22(a). The threshold voltages of transistors M_S and M_L will no longer be the same, and we will indicate the different values by V_{TNS} and V_{TNL}, respectively.

For the design of the saturated load inverter, we use the same circuit conditions that were used for the case of the resistive load ($I_{DD} = 50$ μA with $V_{DD} = 5$ V and $V_L = 0.25$ V). We first choose the W/L ratio of M_L to limit the operating current and power in the inverter. Because M_L is forced to operate in saturation by the circuit connection, its drain current is given by

$$i_D = \frac{K_n'}{2}\left(\frac{W}{L}\right)_L (v_{GS} - V_{TNL})^2 \tag{6.21}$$

For the circuit conditions in Fig. 6.23, load device M_L has $v_{GS} = 4.75$ V when $v_O = 0.25$ V.

Before we can calculate W/L, we must find the value of threshold voltage V_{TNL}, which is determined by the body effect relation represented by Eq. (4.26) in Chapter 4:

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right) \tag{6.22}$$

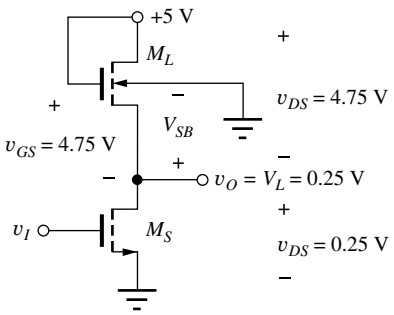


Figure 6.23 Saturated load inverter with $v_O = V_L$.

TABLE 6.8

	NMOS ENHANCEMENT-MODE DEVICE PARAMETERS	NMOS DEPLETION-MODE DEVICE PARAMETERS
V_{TO}	1 V	−3 V
γ	0.5 $\sqrt{\text{V}}$	0.5 $\sqrt{\text{V}}$
$2\phi_F$	0.6 V	0.6 V
K_n'	25 μA/V^2	25 μA/V^2

where V_{TO} = zero bias value of V_{TN} (V)
γ = body effect parameter ($\sqrt{\text{V}}$)
$2\phi_F$ = surface potential parameter (V)

For the rest of the discussion in this chapter, we use the set of device parameters given in Table 6.8.

For the load transistor, we have

$$v_{SB} = v_S - v_B = 0.25\ \text{V} - 0\ \text{V} = 0.25\ \text{V}$$

and

$$V_{TNL} = 1 + 0.5\left(\sqrt{0.25 + 0.6} - \sqrt{0.6}\right) = 1.07\ \text{V}$$

Now, we can find the W/L ratio for the load transistor:

$$\left(\frac{W}{L}\right)_L = \frac{2i_D}{K_n'(v_{GS} - V_{TN})^2} = \frac{2 \cdot 50\ \mu\text{A}}{25\dfrac{\mu\text{A}}{\text{V}^2}(4.75 - 1.07)^2} = \frac{1}{3.39} \tag{6.23}$$

Note that the length of this load device is larger than its width. In most digital IC designs, one of the two dimensions will be made as small as possible corresponding to the minimum feature size in one direction. The W/L ratio is usually written with the smallest number normalized to unity. For $F = 1$ μm, the gate area of M_L is now only 3.52 μm^2, which is comparable to the area of M_S.

6.7.1 Calculation of V_H

Unfortunately, the use of the saturated load device has a detrimental effect on other characteristics of the logic gate. The value of V_H will no longer be equal to V_{DD}. In order to understand this effect, it is helpful to imagine a capacitive load attached to the logic gate, as in Fig. 6.24. Consider the logic gate with $v_I = V_L$ so that M_S is turned off. When M_S turns off, load device M_L charges capacitor C until the current through M_L becomes zero, which occurs when $v_{GS} = V_{TN}$:

$$v_{GS} = V_{DD} - V_H = V_{TN} \qquad \text{or} \qquad V_H = V_{DD} - V_{TN} \tag{6.24}$$

Thus, for the NMOS inverter using a saturated load, the output voltage reaches a maximum value equal to one threshold voltage drop below the power supply voltage V_{DD}. Without body effect, the output would reach $V_H = 5 - 1 = 4$ V. Compared to the original inverter with a resistive load, the high output level is degraded from 5 V to 4 V.

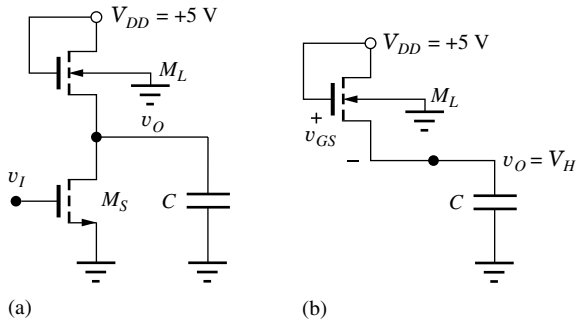


Figure 6.24 (a) Inverter with load capacitance. (b) High output level is reached when $v_I = V_L$ and M_S is off.

Body effect makes the situation even worse. As the output voltage increases toward V_H, v_{SB} increases, the threshold voltage increases above V_{TO} (see Eq. 6.22), and the steady-state value of V_H is less than 4 V. When v_O reaches V_H, this relationship must be true because $v_{SB} = V_H$:

$$V_H = V_{DD} - V_{TNL} = V_{DD} - \left[V_{TO} + \gamma\left(\sqrt{V_H + 2\phi_F} - \sqrt{2\phi_F}\right)\right] \tag{6.25}$$

V_H is found using this quadratic formula

$$V_H = \frac{B - \sqrt{B^2 - 4C}}{2} \qquad \text{with}$$
$$B = 2\left[V_{DD} - V_{TO} + \gamma\sqrt{2\phi_F} + \frac{\gamma^2}{2}\right] \quad \text{and} \quad C = (V_{DD} - V_{TO})^2 + 2\gamma\sqrt{2\phi_F}(V_{DD} - V_{TO}) \tag{6.26}$$

Using Eq. (6.25) with the parameters from Table 6.8 and $V_{DD} = 5$ V, we can solve for V_H, which yields the following quadratic equation:

$$\left(V_H - 4 - 0.5\sqrt{0.6}\right)^2 = 0.25(V_H + 0.6)$$

Solving for V_H gives

$$V_H = 3.39\text{ V},\ \cancel{5.64}\text{ V}$$

In this circuit, the steady-state value of V_H cannot exceed the power supply voltage V_{DD} (actually it cannot exceed $V_{DD} - V_{TNL}$), so the answer must be $V_H = 3.39$ V. We can check our result for V_{OH} by computing the threshold voltage of the load device using Eq. (6.22):

$$V_{TNL} = 1\text{ V} + 0.5\sqrt{\text{V}}\left(\sqrt{(3.39 + 0.6)\text{ V}} - \sqrt{0.6\text{ V}}\right) = 1.61\text{ V}$$

and

$$V_H = V_{DD} - V_{TNL} = 5 - 1.61 = 3.39\text{ V} \quad \checkmark$$

which checks with the previous calculation of V_H.

6.7.2 Calculation of $(W/L)_S$

Now we are in a position to complete the inverter design by calculating W/L for the switching transistor. The bias conditions for $v_O = V_L$ appear in Fig. 6.25 in which the drain current of M_S must equal the design value of 50 μA. For $V_{GS} = 3.39$ V, $V_{DS} = 0.25$ V, and $V_{TNS} = 1$ V, the

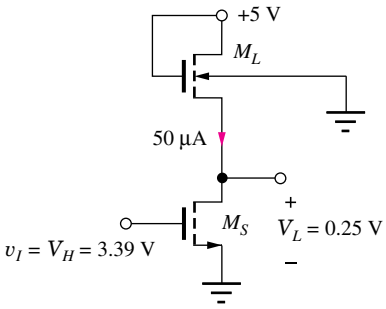
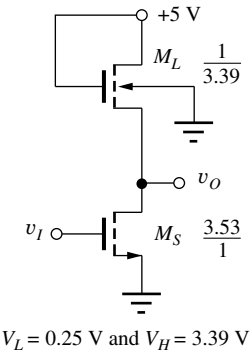


Figure 6.25 Bias conditions used to determine $(W/L)_S$.



V_L = 0.25 V and V_H = 3.39 V

Figure 6.26 Inverter design with saturated load devices.

switching transistor is operating in the triode region. Therefore,

$$i_D = K_n' \left(\frac{W}{L}\right)_S \left(v_{GS} - V_{TNS} - \frac{v_{DS}}{2}\right) v_{DS}$$

$$50\ \mu\text{A} = 25\frac{\mu\text{A}}{\text{V}^2} \left(\frac{W}{L}\right)_S \left(3.39 - 1 - \frac{0.25}{2}\right) 0.25\ \text{V}^2$$

$$\left(\frac{W}{L}\right)_S = \frac{3.53}{1}$$

The final inverter design appears in Fig. 6.26 in which $(W/L)_S = 3.53/1$ and $(W/L)_L = 1/3.39$. The size of the switching device has been increased over that of the resistive load case to compensate for the reduced logic high level of 3.39 V.

EXERCISE: Find V_H for the inverter in Fig. 6.22(a) if $V_{TO} = 0.75$ V. Assume the other parameters remain constant.

ANSWER: 3.60 V

EXERCISE: (a) What value of $(W/L)_S$ is required to achieve $V_L = 0.15$ V in Fig. 6.25? Assume that $i_D = 50\ \mu$A. What is the new value of V_{TNL} for $v_O = V_L$? What value of $(W/L)_L$ is required to set $i_D = 50\ \mu$A for $V_L = 0.15$ V? (b) Repeat for $V_L = 0.10$ V.

ANSWER: (a) 5.76/1, 1.05 V, 1/3.61; (b) 8.55/1, 1.03 V, 1/3.74

Figure 6.27 shows the results of SPICE simulation of the voltage transfer function for the final design in Fig. 6.26. For low values of input voltage, the output is constant at 3.4 V. As the input voltage increases, the slope of the transfer function abruptly changes at the point at which the switching transistor begins to conduct, as the input voltage exceeds the threshold voltage of M_S. As the input voltage continues to increase, the output voltage decreases rapidly and ultimately reaches the design value of 0.25 V for an input of 3.4 V.

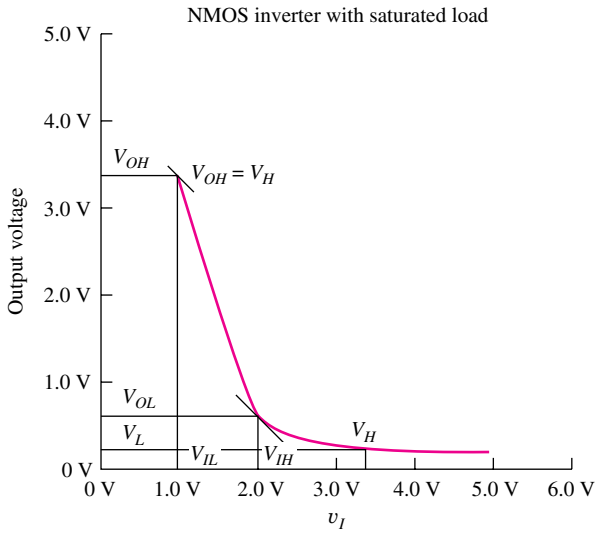


Figure 6.27 SPICE simulation of the voltage transfer function for the NMOS inverter with saturated load.

DESIGN NOTE

STATIC LOGIC INVERTER DESIGN STRATEGY

1. Given design values of V_{DD}, V_L, and the power level, find I_{DD} from V_{DD} and power.
2. Assume switching transistor M_S is off, and find the high output voltage level V_H.
3. Apply V_H to the inverter input and calculate $(W/L)_S$ of the switching transistor based upon design values of V_L and I_{DD}.
4. Calculate load resistor value or $(W/L)_L$ for the load transistor based on design values of V_L and I_{DD}.
5. Check operating region assumptions for M_S and M_L for $v_O = V_L$.
6. Check overall design with SPICE simulation.

DESIGN EXAMPLE 6.5

DESIGN OF AN INVERTER EMPLOYING A SATURATED LOAD DEVICE

Now let's design a saturated load inverter to operate from a 3.3-V supply including the influence of body effect on the transistor design.

PROBLEM Design a saturated load inverter similar to that of Fig. 6.26 with $V_{DD} = 3.3$ V and $V_L = 0.2$ V. Assume $I_{DD} = 30$ μA, $K_n' = 25$ μA/V^2, $V_{TN} = 0.75$ V, $\gamma = 0.5\ \sqrt{\text{V}}$, and $2\phi_F = 0.6$ V.

SOLUTION **Known Information and Given Data:** Circuit topology in Fig. 6.26; $V_{DD} = 3.3$ V, $I_{DD} = 30$ μA, $V_L = 0.2$ V, $K_n' = 25$ μA/V^2, $V_{TO} = 0.75$ V, $\gamma = 0.5\ \sqrt{\text{V}}$, and $2\phi_F = 0.6$ V

Unknowns: W/L ratios of the load and switching transistors M_S and M_L

Approach: First determine V_H including the influence of body effect on the load transistor threshold voltage by evaluating Eq. (6.25). Use V_H, and the specified values of V_L and I_D to find $(W/L)_S$. Use I_D and the voltages in the circuit to find $(W/L)_L$.

Assumptions: M_S is off for $v_I = V_L$. For $v_O = V_L$, M_S is in the triode region, and M_L is in the saturation region.

Analysis: For the values associated with this technology, Eq. (6.25) becomes

$$V_H = 3.3 - \left[0.75 + 0.5\left(\sqrt{V_H + 0.6} - \sqrt{0.6}\right)\right]$$

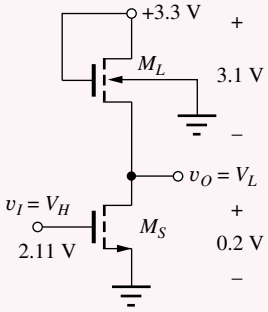
and rearranging this equation gives

$$V_H^2 - 6.125V_H + 8.476 = 0 \qquad \text{for which} \qquad V_H = 2.11\ V,\ \sout{4.01\ V}$$

Since, V_H cannot exceed V_{DD}, the correct choice must be $V_H = 2.11$ V. Note that an extra digit was included in the calculation to increase the precision of the result.

The transistor operating conditions for the load and switching transistors appear in the circuit below for $v_O = V_L$. The triode region expression for the switching transistor drain current with $v_I = V_H$ and $v_O = V_L$ is

$$I_{DS} = K_n'\left(\frac{W}{L}\right)_S\left(V_H - V_{TN} - \frac{V_L}{2}\right)V_L$$



Equating this expression to the drain current yields

$$30\ \mu\text{A} = (25 \times 10^{-6})\left(\frac{W}{L}\right)_S\left(2.11 - 0.75 - \frac{0.2}{2}\right)0.2 \rightarrow \left(\frac{W}{L}\right)_S = \frac{4.76}{1}$$

To find the W/L ratio for the load device, the saturation region expression is evaluated at a drain current of 30 μA. We must recalculate the threshold voltage since the body voltage of the load is 0.2 V when $v_O = V_L = 0.2$ V.

$$I_{DL} = \frac{K_n'}{2}\left(\frac{W}{L}\right)_L(V_{GSL} - V_{TNL})^2$$

$$V_{TNL} = 0.75 + 0.5\left(\sqrt{0.2 + 0.6} - \sqrt{0.6}\right) = 0.81\ \text{V}$$

$$30\ \mu\text{A} = \frac{25\frac{\mu\text{A}}{\text{V}^2}}{2}\left(\frac{W}{L}\right)_L(3.3 - 0.2 - 0.81)^2 \rightarrow \left(\frac{W}{L}\right)_L = \frac{1}{2.19}$$

Our completed design values are $(W/L)_S = 4.76/1$ and $(W/L)_L = 1/2.19$.

Check of Results: We must check the triode and saturation region assumptions for the two MOSFETs: For the switch, $V_{GS} - V_{TN} = 2.11 - 0.75 = 1.36$ V, which is greater than $V_{DS} = 0.2$ V, and the triode region assumption is correct. For the load device, $V_{GS} - V_{TN} = 3.1 - 0.81 = 2.29$ V and $V_{DS} = 3.1$ V, which is consistent with the saturation region of

operation. We can double check our V_H calculation by using it to find the threshold of M_L:

$$V_{TNL} = 0.75 + 0.5\left(\sqrt{2.11 + 0.6} - \sqrt{0.6}\right) = 1.19 \text{ V}$$

This is correct since $V_H + V_{TNL} = 2.11 + 1.19 = 3.3$ V, which must equal the value of V_{DD}.

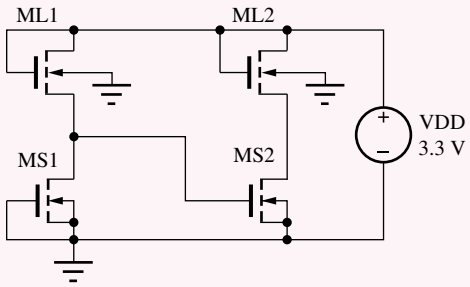
Let us also double check the values of W/L by using them to recalculate the drain currents:

$$I_D = (25 \times 10^{-6})\left(\frac{4.76}{1}\right)\left(2.11 - 0.75 - \frac{0.2}{2}\right)0.2 = 30.0\ \mu\text{A} \quad \checkmark$$

$$I_{DL} = \frac{25\frac{\mu\text{A}}{\text{V}^2}}{2}\left(\frac{1}{2.19}\right)(3.3 - 0.2 - 0.81)^2 = 29.9\ \mu\text{A} \quad \checkmark$$

Both results agree within round off error.

Computer-Aided Analysis: To verify our design with SPICE, we draw the circuit with a schematic capture tool. Two inverters are cascaded in order to get both V_H and V_L with one simulation. The NMOS transistors use the LEVEL = 1 model with KP = 2.5E-5, VTO = 0.75 V, GAMMA = 0.5, and PHI = 0.6 V. The transistor sizes are specified as W = 4.76 U and L = 1 U for M_S, and W = 1 U and L = 2.19 U for M_L. SPICE dc analysis gives $V_H = 2.11$ V and $V_L = 0.196$ V. The drain current of transistor M_{S2} is 30.1 μA. All the values agree with the design specifications.



EXERCISE: Redesign the inverter in Ex. 6.5 to have $V_L = 0.1$ V.

ANSWER: $(W/L)_S = 9.16/1$; $(W/L)_L = 1/2.44$ (Note $V_{TNL} = 0.871$ V)

EXAMPLE 6.6 LOGIC LEVEL ANALYSIS FOR THE SATURATED LOAD INVERTER

Designing our own inverter involves a somewhat different thought process than finding the logic levels associated with someone else's design. Here we find V_H and V_L for a specified inverter design.

PROBLEM Find the high and low logic levels and the power supply current for a saturated load inverter with $(W/L)_S = 10/1$ and $(W/L)_L = 2/1$. The inverter operates with $V_{DD} = 2.5$ V. Assume $K_n' = 25\ \mu\text{A/V}^2$, $V_{TN} = 0.60$ V, $\gamma = 0.5\ \sqrt{\text{V}}$, and $2\phi_F = 0.6$ V.

SOLUTION **Known Information and Given Data:** Circuit topology in Fig. 6.26; $V_{DD} = 2.5$ V, $(W/L)_S = 10/1$, $(W/L)_L = 2/1$, $K_n' = 25\ \mu\text{A/V}^2$, $V_{TO} = 0.60$ V, $\gamma = 0.5\ \sqrt{\text{V}}$, and $2\phi_F = 0.6$ V.

Unknowns: V_H, V_L, and I_{DD} for both logic states

Approach: First, determine V_H. Include the influence of body effect on the load transistor threshold voltage by solving Eq. (6.25). Use V_H and the specified transistor parameters to find V_L by equating the drain currents in the switching and load transistors. Use V_L to find the I_{DS}.

Assumptions: M_S is off for $v_I = V_L$. For $v_O = V_L$, M_S operates in the triode region, and M_L is in the saturation region.

Analysis: First we find V_H, and then we use it to find V_L. For the values associated with this technology, Eq. (6.25) becomes

$$V_H = 2.5 - \left[0.60 + 0.5\left(\sqrt{V_H + 0.6} - \sqrt{0.6}\right)\right]$$

Rearranging this equation gives

$$V_H^2 - 4.824V_H + 5.082 = 0 \qquad \text{for which} \qquad V_H = \text{~~3.00 V~~ or } 1.55 \text{ V}$$

Since, V_H cannot exceed V_{DD}, the correct choice must be $V_H = 1.55$ V. Note that an extra digit was included in the calculation to increase the precision of the result. Since M_S is off, there is no path for current from V_{DD} and $I_{DD} = 0$ for $v_O = V_H$.

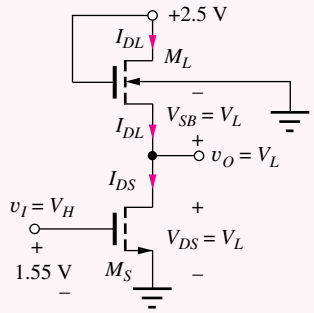
At this point we should check our result to avoid propagation of errors in our calculations. We can use V_H to find V_{TNL} and see if it is consistent with the value of V_H:

$$V_{TNL} = 0.60 + 0.5\left(\sqrt{1.55 + 0.6} - \sqrt{0.6}\right) = 0.946 \text{ V}$$

$$V_H = 2.5 - 0.946 = 1.55 \text{ V}$$

We see that the value of V_H is correct.

To find V_L, we use the condition that I_{DS} must equal I_{DL} in the steady state. The load transistor is saturated by connection, and we expect the switching transistor to be in the triode region since its drain-source voltage should be small. ($V_{DS} = V_L$.)



For $I_{DS} = I_{DL}$, we have $K_n'\left(\frac{10}{1}\right)\left(V_{GSS} - V_{TNS} - \frac{V_L}{2}\right)V_L = \frac{K_n'}{2}\left(\frac{2}{1}\right)(2.5 - V_L - V_{TNL})^2$

where $$V_{TNL} = 0.60 + 0.5\left(\sqrt{V_L + 0.6} - \sqrt{0.6}\right)$$

From the circuit shown, $V_{GSS} = 1.55$ V and $V_{TNS} = 0.60$ V, since there will be no body effect in M_S. Unfortunately, V_{TNL} is a function of the unknown voltage V_L, since the source-bulk voltage of M_L is equal to V_L.

Approach 1: Since we expect V_L to be small, its effect on V_{TNL} will also be small, and one approach to finding V_L is to simply ignore body effect in the load transistor. For this case, equating I_{DS} and I_{DL} gives

$$K_n'\left(\frac{10}{1}\right)\left(1.55-0.6-\frac{V_L}{2}\right)V_L=\frac{K_n'}{2}\left(\frac{2}{1}\right)(2.5-V_L-0.6)^2$$

which can be rearranged to yield a quadratic equation for which

$$V_L = \cancel{1.80\ \text{V}},\ 0.33\ \text{V}$$

$V_L = 0.33$ V since the other root is not consistent with the assumed regions of operation of the transistors. For this value of V_L, the current in M_S is

$$I_{DS}=\left(25\frac{\mu\text{A}}{\text{V}^2}\right)\left(\frac{10}{1}\right)\left(1.55-0.6-\frac{0.33}{2}\right)(0.33)\ \text{V}^2=64.8\ \mu\text{A}$$

Approach 2: For a more exact result, we can find the simultaneous solution to the drain current and threshold voltage equations with the solver in a calculator, with a spreadsheet, or by direct iteration. The result is $V_L = 0.290$ V with $V_{TNL} = 0.68$ V. Using the value of V_L, we can find the current in M_S:

$$I_{DS}=\left(25\frac{\mu\text{A}}{\text{V}^2}\right)\left(\frac{10}{1}\right)\left(1.55-0.6-\frac{0.29}{2}\right)(0.29)\ \text{V}^2=58.4\ \mu\text{A}$$

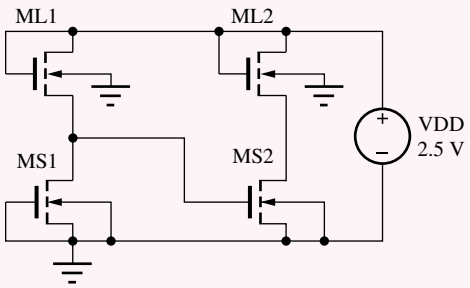
The approximate values in Approach 1 over estimate the more exact values in Approach 2 by approximately 10 percent. In most cases, this would be a negligible error.

Check of Results: Note that we double checked the value of V_H earlier. For V_L, we should check our triode and saturation region assumptions for the two MOSFETs: For the switching transistor, $V_{GS}-V_{TN} = 1.55-0.6 = 0.96$ V, which is greater than $V_{DS} = 0.29$ V, and the triode region assumption is correct. For the load device, $V_{GS} - V_{TN} = 2.5 - 0.29 - 0.68 = 1.53$ V and $V_{DS} = 2.5 - 0.29 = 2.21$, which are consistent with the saturation region of operation. We can further check our results by finding the drain current in M_L:

$$I_{DL}=\left(\frac{25}{2}\frac{\mu\text{A}}{\text{V}^2}\right)\left(\frac{2}{1}\right)(2.5-0.29-0.68)^2=58.5\ \mu\text{A}$$

This value agrees with I_{DS} within round-off error.

Computer-Aided Analysis: To verify our design with SPICE, we draw the circuit with a schematic capture tool. Two inverters are cascaded in order to get both V_H and V_L with one simulation. The gate of MS1 is grounded to force MS1 to be off. The NMOS transistors use the LEVEL = 1 model with KP = 2.5E-5, VTO = 0.60 V, GAMMA = 0.5, and PHI = 0.6 V. The transistor sizes are specified as W = 10 U and L = 1 U for M_S, and W = 2 U and L = 1 U for M_L. SPICE dc analysis gives $V_H = 1.55$ V and $V_L = 0.289$ V. The current in V_{DD} is 58.3 μA. All the values agree with the hand calculations.



EXERCISE: Use the "Solver" on your calculator to find V_H in Ex. 6.6.

EXERCISE: Repeat the calculations with $\gamma = 0$. Check your results with SPICE.

ANSWERS: 1.90 V; 0 A; 0.235 V; 69.3 μA

6.7.3 NOISE MARGIN ANALYSIS

We now explore the values of V_{IL}, V_{OL}, V_{IH}, and V_{OH} for the inverter with a saturated load device. Remember that these voltages are defined by the points in the transfer function at which the slope is equal to -1. In Fig. 6.27, the slope of the transfer function abruptly changes as M_S begins to conduct at the point where $v_I = V_{TNS}$. This point defines V_{IL}:

$$V_{IL} = V_{TNS} = 1 \text{ V} \qquad \text{for } V_{OH} = V_H = V_{DD} - V_{TNL} = 3.4 \text{ V} \tag{6.27}$$

Next let us find V_{IH} and V_{OL}. To find a relationship between v_I and v_O, we observe that the drain currents in the switching and load devices must be equal. At $v_I = V_{IH}$, the input is at a relatively high voltage and the output is at a relatively low voltage. Thus, we can guess that M_S will be in the triode region, and we already know that the circuit connection forces M_L to operate in the saturation region. Equating drain currents in the switching and load transistors:

$$\begin{gathered} i_{DS} = i_{DL} \\ K_S\left(v_I - V_{TNS} - \frac{v_O}{2}\right)v_O = \frac{K_L}{2}(V_{DD} - v_O - V_{TNL})^2 \\ K_S = K_n'\left(\frac{W}{L}\right)_S \qquad \text{and} \qquad K_L = K_n'\left(\frac{W}{L}\right)_L \end{gathered} \tag{6.28}$$

The point of interest is $dv_O/dv_I = -1$. Solving for the corresponding value of v_O is fairly involved, so we will state the results here. The detailed calculations can be found on the **MCD website.**

$$V_{OL} = \frac{V_{DD} - V_{TNL}}{\sqrt{1 + 3K_R}} \quad \text{with} \quad V_{TNL} = V_{TO} + \gamma\left(\sqrt{V_{OL} + 2\phi_F} - \sqrt{2\phi_F}\right) \quad \text{and} \quad K_R = \frac{(W/L)_S}{(W/L)_L}$$

$$V_{IH} = V_{TNS} + \frac{V_{OL}}{2} + \frac{(V_{DD} - V_{OL} - V_{TNL})^2}{2K_R V_{OL}} \tag{6.29}$$

Substituting the values from our saturated load inverter design gives

$$V_{OL} = \frac{5 - V_{TNL}}{\sqrt{1 + 3(3.53)(3.39)}} \qquad \text{with} \qquad V_{TNL} = 1 + 0.5\left(\sqrt{V_{OL} + 0.6} - \sqrt{0.6}\right)$$

These equations can be rearranged into a quadratic equation just as was done to find V_H for the saturated load inverter, but here we will use an iterative update process to find the solution to these equations with our calculator or a spreadsheet. The steps in the iteration process are

1. Choose a starting guess for V_{OL}.
2. Calculate the corresponding value of V_{TNL}.

3. Update the value of V_{OL}.
4. Repeat steps 2 and 3 until convergence is obtained.

Table 6.9 provides an example of the iteration process for the inverter design in Fig. 6.26 with $K_R = 3.53(3.39) = 12.0$.

TABLE 6.9

ITERATION NUMBER	V_{OL}	V_{TNL}	V'_{OL}
1	0.5000	1.1371	0.6359
2	0.6359	1.1686	0.6307
3	0.6307	1.1674	0.6309
4	0.6309	1.1674	0.6309

Thus we have $V_{OL} = 0.63$ V with $V_{TNL} = 1.17$ V, and these values are used to find V_{IH}.

$$V_{IH} = 1 + \frac{0.63}{2} + \frac{(5 - 0.63 - 1.17)^2}{2(3.53)(3.39)(0.63)} = 1.99 \text{ V}$$

The values of V_{IH} and V_{OL} agree well with the transfer characteristic simulation results in Fig. 6.27. The noise margins are given by

$$\text{NM}_L = V_{IL} - V_{OL} = 1 - 0.63 = 0.37 \text{ V}$$

$$\text{NM}_H = V_{OH} - V_{IH} = 3.39 - 1.99 = 1.40 \text{ V}$$

Compared to the inverter with the resistor load, the value of NM_L is unchanged, but the value of NM_H has deteriorated because of the reduction of the high output level V_H. In Eq. (6.29), K_R compares the transconductance of M_S to that of M_L, and we see that the noise margins improve as the value of K_R increases.

EXAMPLE 6.7 NOISE MARGIN CALCULATION FOR THE SATURATED LOAD INVERTER

Use the results of the noise margin analysis to find numerical values of the noise margins for the 3.3-V saturated load inverter design from the last example.

PROBLEM Calculate the noise margins for the inverter in Design Example 6.5.

SOLUTION **Known Information and Given Data:** The NMOS saturated load inverter circuit in Design Ex. 6.5 with $V_{DD} = 3.3$ V, $(W/L)_S = 4.76/1$, $(W/L)_L = 1/2.19$, $K'_n = 25\ \mu\text{A/V}^2$, $V_{TO} = 0.75$ V, $\gamma = 0.5$, and $2\phi_F = 0.6$ V

Unknowns: The values of V_{IL}, V_{OH}, V_{IH}, V_{OL}, NM_L, NM_H

Approach: Use the given data to evaluate Eqs. (6.29); use the results to find the noise margins: $\text{NM}_H = V_{OH} - V_{IH}$ and $\text{NM}_L = V_{IL} - V_{OL}$

Assumptions: Equation (6.28) assumes M_L is in the saturation region and M_S is in the triode region. Assume $V_{IL} = V_{TNS}$ and $V_{OH} = V_H$ as in Fig. 6.27.

Analysis: Based on these assumptions, noting that $V_{TNS} = V_{TO} = 0.75$ V, and finding $V_H = 2.11$ V in Ex. 6.6, we have

$$V_{IL} = 0.75 \text{ V} \qquad \text{and} \qquad V_{OH} = V_H = 2.11 \text{ V}$$

To find V_{OL} and V_{IH}, we first need to find the simultaneous solution to Eq. (6.29)

$$V_{OL} = \frac{V_{DD} - V_{TNL}}{\sqrt{1 + 3K_R}} = \frac{3.3 - V_{TNL}}{\sqrt{1 + 3(4.76)(2.19)}} = \frac{3.3 - V_{TNL}}{5.68}$$

and the threshold voltage expression for the load device.

$$V_{TNL} = 0.75 + 0.5\left(\sqrt{V_{OL} + 0.6} - \sqrt{0.6}\right)$$

Using our calculator or computer to help find the solution gives $V_{OL} = 0.428$ V with $V_{TNL} = 0.870$ V. V_{IH} can now be calculated:

$$V_{IH} = V_{TNS} + \frac{V_{OL}}{2} + \frac{(V_{DD} - V_{OL} - V_{TNL})^2}{2K_R V_{OL}}$$

$$V_{IH} = 0.75 + \frac{0.43}{2} + \frac{(3.3 - 0.43 - 0.87)^2}{2(2.19)(4.76)(0.43)} = 1.41 \text{ V}$$

Using the values just calculated, the noise margins are

$$\text{NM}_H = V_{OH} - V_{IH} = 2.1 - 1.41 = 0.69 \text{ V}$$

and

$$\text{NM}_L = V_{IL} - V_{OL} = 0.75 - 0.43 = 0.32 \text{ V}$$

Check of Results: The noise margins are smaller than those calculated for the inverter in Fig. 6.26(b), that was designed with a 5-V power supply but appear reasonable. We need to check the assumptions underlying Eq. (6.29). For V_{IH} and V_{OL},

For M_S: $$V_{GS} - V_{TN} = V_{IH} - V_{TN} = 1.41 - 0.75 = 0.66 \text{ V}$$

and

$$V_{DS} = V_{OL} = 0.43 \text{ V} \quad \checkmark \text{ Triode region is correct}$$

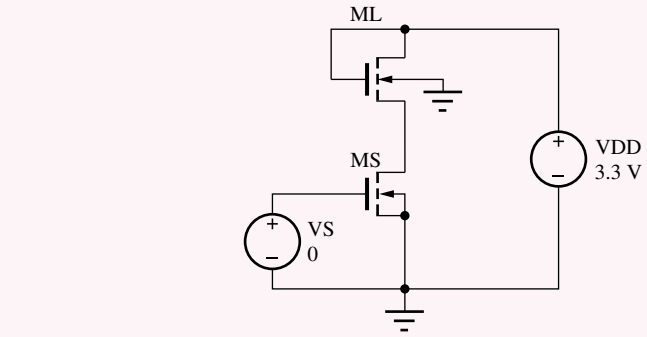
For M_L: $$V_{GS} - V_{TN} = V_{DD} - V_{OL} - V_{TN} = 3.3 - 0.43 - 0.87 = 2.00 \text{ V}$$

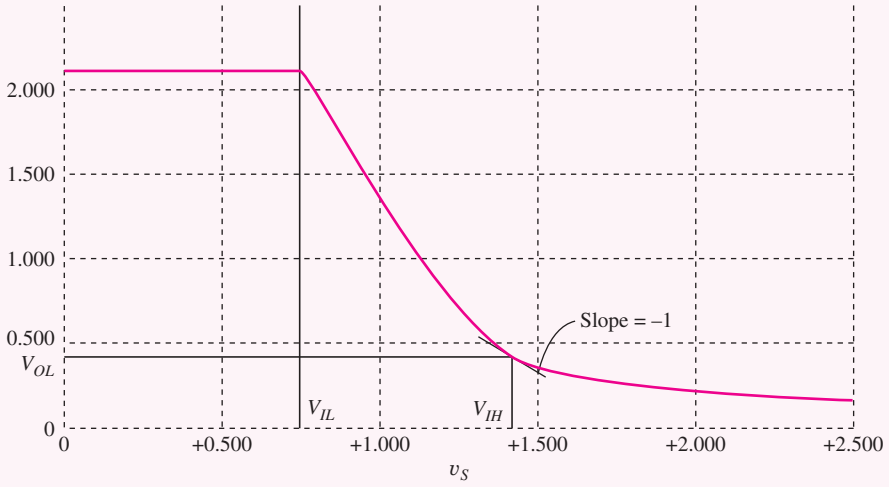
and

$$V_{DS} = V_{DD} - V_{OL} = 3.3 - 0.43 = 2.87 \text{ V} \quad \checkmark \text{ Saturation region is correct}$$

Discussion: Our analysis indicates that a long chain of inverters can tolerate electrical noise and process variations equivalent to 0.32 V in the low input state and 0.69 V in the high state. We again observe that the values of the two noise margins are not equal.

Computer-Aided Analysis: The circuit shown here can be used to find the nose margins by plotting the voltage transfer characteristic for the inverter. A dc sweep analysis is used to change the value of VS from 0 V to 2.5 V in 10 mV steps. The NMOS transistors use the LEVEL = 1 model with KP = 2.5E-5, VTO = 0.75 V, GAMMA = 0.5, and PHI = 0.6 V. The transistor sizes are specified as W = 4.76 U and L = 1 U for M_S, and W = 1 U and L = 2.19 U for M_L. SPICE gives $V_H = 2.11$ V and $V_L = 0.196$ V. The VTC values agree closely with our hand calculations.





EXERCISE: (a) Use your calculator to perform a "trial-and-error" analysis to find V_{OL} and $V_{TNL} = 0.87$ V beginning with a guess of $V_{OL} = 0.80$ V. (b) Verify that $V_{OL} = 0.429$ V and $V_{TNL} = 0.87$ V indeed satisfy the two simultaneous equations in this example.

ANSWERS: V_{OL} sequence: 0.800 V, 0.413 V, 0.429 V, 0.428 V

6.8 NMOS INVERTER WITH A LINEAR LOAD DEVICE

Figure 6.21(d) provides a second workable choice for the load transistor M_L. In this case, the gate of the load transistor is connected to a separate voltage V_{GG}. V_{GG} is normally chosen to be at least one threshold voltage greater than the supply voltage V_{DD}:

$$V_{GG} \geq V_{DD} + V_{TNL}$$

For this value of V_{GG}, the output voltage in the high output state V_H is equal to V_{DD}.

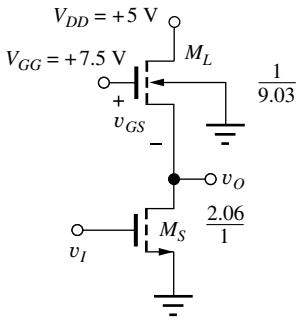


Figure 6.28 Linear load inverter design.

The region of operation of M_L in Fig. 6.28 can be found by comparing $V_{GS} - V_{TNL}$ to V_{DS}. For the load device with its output at v_O and $V_{GG} \geq V_{DD} + V_{TNL}$:

$$\begin{aligned} v_{GS} - V_{TNL} &= V_{GG} - v_O - V_{TNL} \\ &\geq V_{DD} + V_{TNL} - v_O - V_{TNL} \\ &\geq V_{DD} - v_O \end{aligned} \tag{6.30}$$

So $v_{GS} - V_{TNL} \geq V_{DD} - v_O$, but $v_{DS} = V_{DD} - v_O$, which demonstrates that the load device always operates in the triode (linear) region.

The W/L ratios for M_S and M_L can be calculated using methods similar to those in the previous sections; the results are shown in Fig. 6.28. Because V_H is now equal to $V_{DD} = 5$ V, M_S is again 2.06/1. However, for $v_O = V_L$, v_{GS} of M_L is large, and $(W/L)_L$ must be reduced to (1/9.03) in order to limit the current to the desired level. (Verification of these values is left for Prob. 6.76.)

Introduction of the additional power supply voltage V_{GG} overcomes the reduced output voltage problem associated with the saturated load device. However, the cost of the additional power supply level as well as the increased wiring congestion introduced by distribution of the extra supply voltage to every logic gate cause this form of load topology to be used rarely.

6.9 NMOS INVERTER WITH A DEPLETION-MODE LOAD

The saturated load and linear load circuits were developed for use in integrated circuits because all the devices had the same threshold voltages in early NMOS and PMOS technologies. However, once ion-implantation technology was perfected, it became possible to selectively adjust the threshold of the load transistors to alter their characteristics to become those of NMOS depletion-mode devices with $V_{TN} < 0$, and the use of the circuit in Fig. 6.29 became feasible.

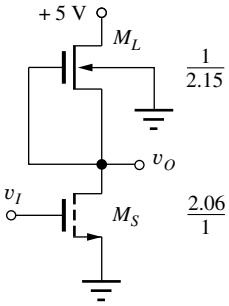


Figure 6.29 NMOS inverter with depletion-mode load.

The circuit topology for the NMOS inverter with a depletion-mode load device is shown in Fig. 6.29. Because the threshold voltage of the NMOS depletion-mode device is negative, a channel exists even for $v_{GS} = 0$, and the load device conducts current until its drain-source voltage becomes zero. When the switching device M_S is off ($v_I = V_L$), the output voltage rises to its final value of $V_H = V_{DD}$.

For $v_I = V_{OH}$, the output is low at $v_O = V_L$. In this state, current is limited by the depletion-mode load device, and it is normally designed to operate in the saturation region, requiring:

$$v_{DS} \geq v_{GS} - V_{TNL} = 0 - V_{TNL} \qquad \text{or} \qquad v_{DS} \geq -V_{TNL}$$

6.9.1 Design of the W/L Ratio of M_L

As an example of inverter design, if we assume $V_{DD} = 5$ V, $V_L = 0.25$ V, and $V_{TNL} = -3$ V, then the operating voltage for the load device with $v_O = V_L$ is $V_{DS} = 4.75$ V, which is greater than $-V_{TNL} = 3$ V, and the MOSFET operates in the saturation region. The drain current of the depletion-mode load device operating in the saturation region with $V_{GS} = 0$ is given by

$$i_{DL} = \frac{K_n'}{2}\left(\frac{W}{L}\right)_L (v_{GSL} - V_{TNL})^2 = \frac{K_n'}{2}\left(\frac{W}{L}\right)_L (V_{TNL})^2 \tag{6.31}$$

Just as for the case of the saturated load inverter, body effect must be taken into account in the depletion-mode MOSFET, and we must calculate V_{TNL} before $(W/L)_L$ can be properly determined. For depletion-mode devices, we use the parameters in Table 6.8, and

$$V_{TNL} = -3 \text{ V} + 0.5\sqrt{\text{V}}\left(\sqrt{(0.25 + 0.6)\text{ V}} - \sqrt{0.6\text{ V}}\right) = -2.93 \text{ V}$$

Using the design current of 50 μA with $K_n' = 25\ \mu\text{A/V}^2$ and the depletion-mode threshold voltage of −2.93 V, we find

$$(W/L)_L = 0.466/1 = 1/2.15$$

6.9.2 Design of the W/L Ratio of M_S

When $v_I = V_H = V_{DD}$, the switching device once again has the full supply voltage applied to its gate, and its W/L ratio will be identical to the design of the NMOS logic gate with resistor load: $(W/L)_S = 2.06/1$. The completed depletion-mode load inverter design appears in Fig. 6.29, and the logic levels of the final design are $V_L = 0.25$ V and $V_H = 5.0$ V.

Figure 6.30 shows the results of SPICE simulation of the voltage transfer function for the final inverter design with the depletion-mode load. For low values of input voltage, the output is 5 V. As the input voltage increases, the slope of the transfer function gradually changes as the switching transistor begins to conduct for an input voltage exceeding the threshold voltage. As the

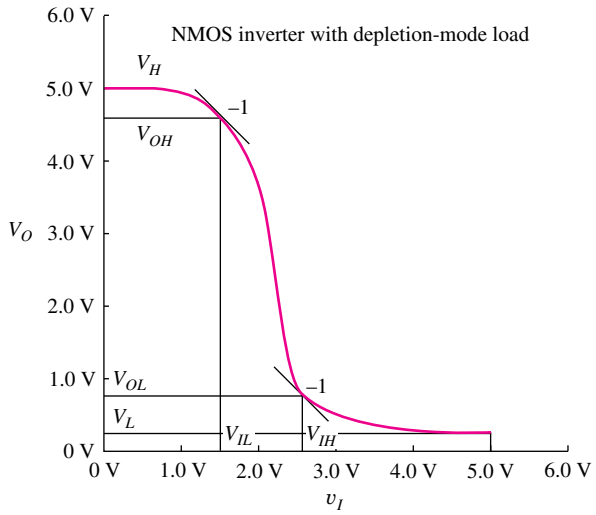


Figure 6.30 SPICE simulation results for the voltage transfer function of the NMOS depletion-load inverter of Fig. 6.29.

input voltage continues to increase, the output voltage decreases rapidly and ultimately reaches the design value of 0.25 V for an input of 5.0 V.

6.9.3 Noise Margins for the Inverter with Depletion-Mode Load

The approach to finding the noise margins for the depletion load inverter is similar to that used for the other NMOS inverters. Again, remember that we are interested in the points in the transfer function at which the slope is −1, and only the results are presented here. The detailed calculations for V_{IL}, V_{OH}, V_{IH}, and V_{OL} can be found on the **MCD website.**

$$V_{OH} = V_{DD} + V_{TNL}\left(1 - \sqrt{\frac{K_R}{1+K_R}}\right) \quad \text{with} \quad V_{TNL} = V_{TO} + \gamma\left(\sqrt{V_{OH} + 2\phi_F} - \sqrt{2\phi_F}\right)$$
$$V_{IL} = V_{TNS} - \frac{V_{TNL}}{\sqrt{K_R^2 + K_R}} \tag{6.32}$$

In these expressions, $K_R = (W/L)_S/(W/L)_L$. The results in Eqs. (6.32) assume that transistor M_S is saturated and that M_L is in the triode region.

$$V_{OL} = \frac{-V_{TNL}}{\sqrt{3K_R}} \quad \text{with} \quad V_{TNL} = V_{TO} + \gamma\left(\sqrt{V_{OL} + 2\phi_F} - \sqrt{2\phi_F}\right)$$
$$V_{IH} = V_{TNS} - \frac{2V_{TNL}}{\sqrt{3K_R}} \tag{6.33}$$

The results in Eqs. (6.33) assume that transistor M_L is saturated and that M_S is in the triode region.

Finding V_{OH} and V_{IL}

The relations for V_{OH} and V_{OL} can each be rearranged into a quadratic equation just as was done in order to find V_H for the saturated load inverter. For the 5-V depletion-mode inverter design, we have $K_R = 2.06(2.15) = 4.43$. Equation set (6.32) becomes

$$V_{OH} = 5 + 0.1V_{TNL} \qquad V_{TNL} = -3 + 0.5\left(\sqrt{V_{OH} + 0.6} - \sqrt{0.6}\right) \qquad V_{IL} = V_{TNS} - \frac{V_{TNL}}{4.90}$$

Solving for V_{OH}, we get this quadratic equation

$$V_{OH}^2 - 9.327V_{OH} + 21.73 = 0$$

and the solution is $V_{OH} = 4.78$ V, $V_{TNL} = -2.23$ V, and $V_{IL} = 1.46$ V. The second root, $V_{OH} = 4.53$ V, does not provide a consistent solution to the original two equations.

As always, the operating region assumptions of the transistors should be checked. For $V_{OH} = 4.78$ V, the values of v_{DS} for M_S and M_L are 4.78 V and 0.22 V, respectively. For, M_S, $v_{GS} - V_{TNS} = 1.46 - 1 = 0.46$ V and $v_{DS} = 4.78$ V. In this case, $v_{DS} > (v_{GS} - V_{TNS})$, so M_S is saturated. ✔ For, M_L, $v_{GS} - V_{TNL} = 0 - (-2.23) = 2.23$ V and $v_{DS} = 0.22$ V. In this case, $v_{DS} < (v_{GS} - V_{TNS})$, so M_L operates in the triode region. ✔ Both regions are consistent with the assumptions used to develop the noise margin equations.

Finding V_{OL} and V_{IH}

Similarly, Eqs. (6.33) become

$$V_{OL} = \frac{-V_{TNL}}{3.65} \qquad V_{TNL} = -3 + 0.5\left(\sqrt{V_{OL} + 0.6} - \sqrt{0.6}\right) \qquad V_{IH} = V_{TNS} - \frac{2V_{TNL}}{3.65}$$

Solving for V_{OL}, we have

$$V_{OL}^2 - 1.877V_{OH} + 0.852 = 0$$

for which the solution is $V_{OL} = 0.769$ V, $V_{TNL} = -2.80$ V, and $V_{IH} = 2.53$ V. Again, the second root, $V_{OL} = 1.108$ V, does not satisfy the two original equations.

Again, the operating region assumptions of the transistors should be checked. For $V_{OL} = 0.79$ V, the values of v_{DS} for M_S and M_L are 0.79 V and 4.21 V, respectively. For, M_S, $v_{GS} - V_{TNS} = 2.53 - 1 = 1.53$ V and $v_{DS} = 0.79$ V. In this case, $v_{DS} < (v_{GS} - V_{TNS})$, so M_S operates in the triode region. ✔ For M_L, $v_{GS} - V_{TNL} = 0 - (-2.80) = 2.80$ V and $v_{DS} = 4.21$ V. In this case, $v_{DS} > (v_{GS} - V_{TNS})$, so M_L is saturated. ✔ Both regions are consistent with the assumptions used to develop the noise margin equations.

NM_L and NM_H

Now, the noise margins can be calculated for the design in Fig. 6.29, using the results just derived:

$$NM_L = V_{IL} - V_{OL} = 1.46 - 0.77 = 0.69 \text{ V}$$
$$NM_H = V_{OH} - V_{IH} = 4.78 - 2.53 = 2.25 \text{ V}$$

Note that the values of calculations for V_{IL}, V_{OH}, V_{IH}, V_{OL}, and the noise margins agree with the simulation results in Fig. 6.30.

Because of its overall advantages, the inverter with the depletion-mode load device became the most widely used form of NMOS logic, so let us explore the noise margins for this circuit in more detail. Figure 6.31 depicts the results of calculations of the noise margins versus the parameter K_R for the inverter with a depletion-mode load. As K_R increases, NM_H monotonically increases, whereas NM_L decreases quickly reaching an almost constant value for $K_R > 3$. The values in the graph agree well with the hand calculations for our inverter design with $K_R = 4.43$. Note that NM_H becomes negative for values of K_R less than approximately 0.9, and the circuit will no longer function properly as a logic inverter.

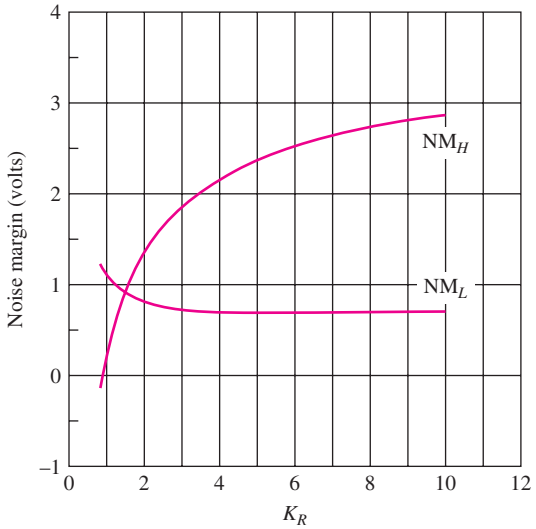


Figure 6.31 Noise margins versus $K_R = K_S/K_L$ for the NMOS inverter with a depletion-mode load. $V_{DD} = 5$ V, $V_{TOS} = 0.75$ V, $V_{TOL} = -3$ V, $\gamma = 0.5$ $V^{0.5}$, and $2\phi_F = 0.6$ V.

EXERCISE: Verify that $V_{OH} = 4.53$ V and $V_{OL} = 1.108$ V do not satisfy their respective equation sets as stated above.

DESIGN EXAMPLE 6.8

NMOS INVERTER WITH DEPLETION-MODE LOAD

Now we will redesign the depletion-load inverter for operation with a lower power supply voltage.

PROBLEM Design the inverter with depletion-mode load of Fig. 6.29 for operation with $V_{DD} = 3.3$ V. Assume $V_{TO} = 0.7$ V for the switching transistor and $V_{TO} = -3$ V for the depletion-mode load. Keep the other design parameters the same (i.e., $V_L = 0.25$ V and $P = 25$ mW.)

SOLUTION **Known Information and Given Data:** Circuit topology in Fig. 6.29; $V_{DD} = 3.3$ V, $P = 25$ mW, $V_L = 0.25$ V, $K_n' = 25\ \mu\text{A/V}^2$, $V_{TOS} = 0.70$ V, $V_{TOL} = -3$ V, $\gamma = 0.5\ \sqrt{\text{V}}$, and $2\phi_F = 0.6$ V for both transistor types

Unknowns: Power supply current I_{DD}, W/L ratios of the load and switching transistors M_S and M_L

Approach: Find V_H. Use V_H, I_{DD}, and the specified value of V_L and to find $(W/L)_S$. Calculate V_{TNL}. Use I_{DD}, V_{TNL}, and the voltages in the circuit to find $(W/L)_L$.

Assumptions: M_S is off for $v_I = V_L$. For $v_O = V_L$, M_S is in the triode region, and M_L is in the saturation region.

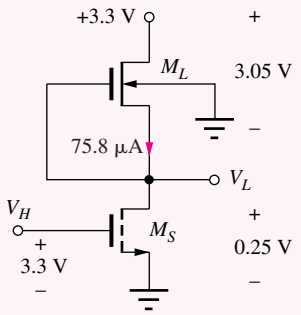
Analysis: First, we need to know the power supply current for $v_O = V_L$ in order to calculate the W/L ratios of both transistors.

$$I_{DD} = \frac{P}{V_{DD}} = \frac{0.25\ \text{mW}}{3.3\ \text{V}} = 75.8\ \mu\text{A}$$

The value of V_H will be equal to V_{DD} as long as the threshold of the depletion-mode device remains negative for $v_O = V_{DD}$. Checking the value of V_{TNL}:

$$V_{TNL} = -3 + 0.5\left(\sqrt{3.3 + 0.6} - \sqrt{0.6}\right) = -2.40\ \text{V} \quad \checkmark$$

Therefore, $V_H = V_{DD} = 3.3$ V. Now the size of the switching transistor can be determined. The transistor has $V_{GS} = V_H = 3.3$ V and $V_{DS} = V_L = 0.25$ V, as shown in the figure.



$$75.8\ \mu\text{A} = 25\ \mu\text{A}\left(\frac{W}{L}\right)_S\left(3.3 - 0.7 - \frac{0.25}{2}\right)0.25 \rightarrow \left(\frac{W}{L}\right)_S = \frac{4.90}{1}$$

In order to design the load transistor, we calculate its threshold voltage with $v_O = V_L = 0.25$ V, and then use V_{TNL} to find W/L (note that $V_{SB} = V_L = 0.25$ V):

$$V_{TNL} = -3 + 0.5\left(\sqrt{0.25 + 0.6} - \sqrt{0.6}\right) = -2.926 \text{ V}$$

$$75.8\ \mu\text{A} = \frac{25\ \mu\text{A}}{2}\left(\frac{W}{L}\right)_L (-2.926)^2 \rightarrow \left(\frac{W}{L}\right)_L = \frac{1}{1.41}$$

Check of Results: We must check the triode and saturation region assumptions for the two MOSFETs. For the switch, $V_{GS} - V_{TN} = 3.3 - 0.70 = 2.6$ V, which is greater than $V_{DS} = 0.25$ V, and the triode region assumption is correct. For the load device, $V_{GS} - V_{TN} = 0 - (-2.96) = 2.96$ V, and $V_{DS} = 3.3 - 0.25 = 3.05$ V, which are consistent with the saturation region of operation. Let us also double check the values of W/L by directly calculating the drain currents:

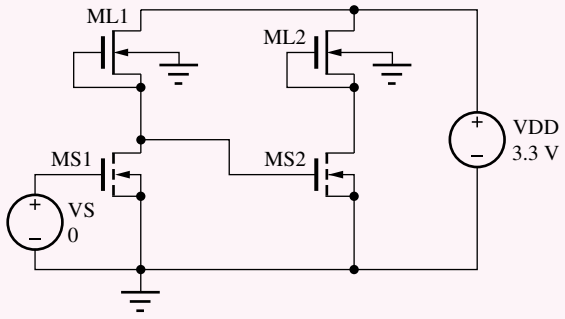
$$I_{DS} = (25 \times 10^{-6})\left(\frac{4.90}{1}\right)\left(3.3 - 0.70 - \frac{0.25}{2}\right)0.25 = 75.8\ \mu\text{A} \quad \checkmark$$

$$I_{DL} = \frac{25\frac{\mu\text{A}}{\text{V}^2}}{2}\left(\frac{1}{1.41}\right)[0 - (-2.926)]^2 = 75.9\ \mu\text{A} \quad \checkmark$$

Both results agree within round-off error.

Discussion: Comparing our new design with that of Fig. 6.29, we find that the reduced value of V_H requires a larger W/L ratio for M_S in order to maintain the required value of V_L at the same operating current. The smaller value of threshold voltage modifies W/L only slightly. The lower value of V_H reduces the body effect in the load device which reduces the value of L required to limit the drain current to the design value.

Computer-Aided Analysis: Let us verify our design with SPICE. Here again, two inverters are cascaded in order to get both V_H and V_L with one simulation. The enhancement-mode transistors use the LEVEL = 1 model with KP = 2.5E-5, VTO = 0.70 V, GAMMA = 0.5, and PHI = 0.6 V. For the depletion mode devices, VTO is changed to VTO = −3 V. The transistor sizes are specified as W = 4.90 U and L = 1 U for M_S, and W = 1 U and L = 1.41 U for M_L. SPICE gives $V_H = 3.30$ V and $V_L = 0.250$ V with $I_D = 75.9\ \mu$A for transistor M_{S2}. All the values confirm our design calculations.



EXERCISE: What are the new W/L ratios for the transistors in Ex. 6.8 if $V_{TOL} = -2$ V?

ANSWERS: $(W/L)_S = 4.90/1$; $(W/L)_L = 1.64/1$

EXAMPLE 6.9 DEPLETION-MODE INVERTER NOISE MARGIN CALCULATION

Use the analysis in Section 6.9 to find numeric values of the noise margins. Compare the results to SPICE simulations.

PROBLEM Calculate the noise margins for the inverter from Design Ex. 6.8. Use SPICE simulation to confirm the noise margin calculations.

SOLUTION **Known Information and Given Data:** Circuit topology in Fig. 6.29; $V_{DD} = 3.3$ V, $P = 25$ mW, $V_L = 0.25$ V, $K_n' = 25\ \mu\text{A/V}^2$, $V_{TOS} = 0.70$ V, $V_{TOL} = -3$ V, $\gamma = 0.5\ \sqrt{\text{V}}$, and $2\phi_F = 0.6$ V for both transistor types; $(W/L)_S = 4.90/1$, $(W/L)_L = 1/1.41$

Unknowns: The values of V_{IL}, V_{OH}, V_{IH}, V_{OL}, NM_L, and NM_H

Approach: Use a computer or calculator to find the solution to Eqs. (6.32) for V_{IL} and V_{OH}, and Eqs. (6.33) for V_{IH} and V_{OL}. Use the results to find the noise margins: $\text{NM}_H = V_{OH} - V_{IH}$ and $\text{NM}_L = V_{IL} - V_{OL}$.

Assumptions: Equations (6.32) are based on the assumptions that M_S is operating in the saturation region and M_L is in the triode region, whereas Eqs. (6.33) assume that M_S is operating in the triode region and M_L is saturated.

Analysis: First, let us find the values of V_{IL} and V_{OH}. We must find values of V_{OH} and V_{TNL} that represent the common solution to Eqs. (6.32). Then V_{TNL} can be used to find the value of V_{IL}. For the inverter design in question, $K_R = 4.90 \cdot 1.41 = 6.91$, and substituting the known data into Eqs. (6.32) gives

$$V_{OH} = 3.3 + V_{TNL}\left(1 - \sqrt{\frac{6.91}{1 + 6.91}}\right) = 3.3 + 0.065 V_{TNL}$$

$$V_{TNL} = -3 + 0.5\left(\sqrt{V_{OH} + 0.6} - \sqrt{0.6}\right)$$

and

$$V_{IL} = 0.70 - \frac{V_{TNL}}{\sqrt{(6.91)^2 + 6.91}} = 0.70 - 0.135 V_{TNL}$$

Using a computer or calculator yields $V_{OH} = 3.14$ V, $V_{TNL} = -2.42$ V, and $V_{IL} = 1.03$ V.

To determine the values of V_{IH} and V_{OL}, a common solution must be found to Eqs. (6.33). Then V_{TNL} can be used to find the value of V_{IH}. Equations (6.33) become

$$V_{OL} = -\frac{V_{TNL}}{\sqrt{3 \cdot 6.91}} = -\frac{V_{TNL}}{4.55}$$

$$V_{TNL} = -3 + 0.5\left(\sqrt{V_{OL} + 0.6} - \sqrt{0.6}\right)$$

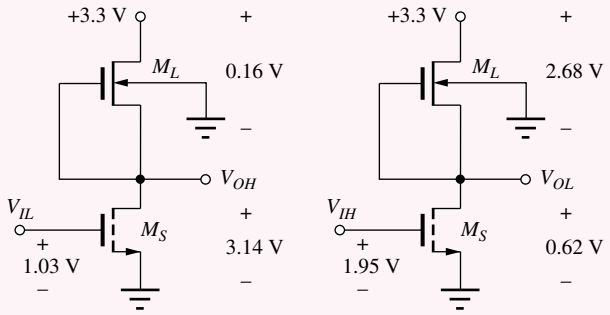
and

$$V_{IH} = 0.70 - \frac{2V_{TNL}}{4.55}$$

Using a computational aid yields $V_{OL} = 0.623$ V, $V_{TNL} = -2.83$ V, and $V_{IH} = 1.95$ V, and the noise margins are

$$\text{NM}_H = V_{OH} - V_{IH} = 3.14 - 1.95 = 1.19 \text{ V}$$
$$\text{NM}_L = V_{IL} - V_{OL} = 1.03 - 0.62 = 0.41 \text{ V}$$

Check of Results: We must check the triode and saturation region assumptions for the two MOSFETs.



For V_{IL} and V_{OH}

M_S: $V_{GS} - V_{TN} = 1.03 - 0.40 = 0.63$ V and $V_{DS} = 3.14$ V $\rightarrow$ Saturated ✔

M_L: $V_{GS} - V_{TN} = 0 - (-2.42) = 2.42$ V and $V_{DS} = 0.16$ V $\rightarrow$ Triode ✔

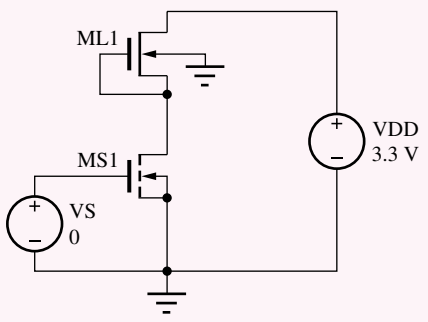
For V_{IH} and V_{OL},

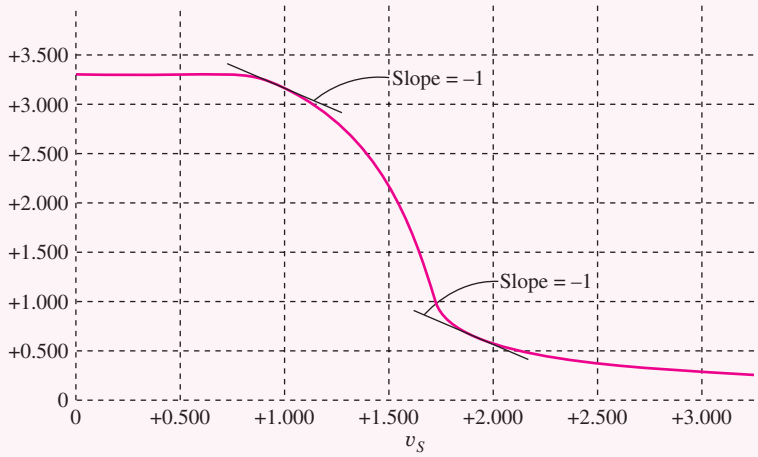
M_S: $V_{GS} - V_{TN} = 1.95 - 0.70 = 1.25$ V and $V_{DS} = 0.62$ V $\rightarrow$ Triode ✔

M_L: $V_{GS} - V_{TN} = 0 - (-2.25) = 2.25$ V and $V_{DS} = 2.68$ V $\rightarrow$ Saturated ✔

Discussion: As a result of this design, we observe that the inverter with the 3.3-V power supply voltage has lower noise margins than the one using the 5-V supply. From an inspection of Eq. (6.32), we see that V_{OH} is directly dependent on V_{DD}.

Computer-Aided Analysis: The circuit below can be used to find the noise margins by plotting the voltage transfer characteristic for the inverter. A dc sweep analysis is used to change the value of VS from 0 V to 3.3 V in 5 mV steps. The transistors use the LEVEL = 1 model with KP = 2.5E-5, GAMMA = 0.5, and PHI = 0.6 V. For M_S, VTO = 0.70 V, and for M_L, VTO = −3 V. The transistor sizes are specified as W = 4.90 U and L = 1 U for M_S, and W = 1 U and L = 1.41 U for M_L. The VTC values from the graph agree well with our hand calculations.





Voltage transfer characteristic for depletion load inverter

EXERCISE: Use quadratic equations instead of numeric iteration to find V_{IL}, V_{OH}, V_{IH}, and V_{OL}.

6.10 NMOS INVERTER SUMMARY AND COMPARISON

Figure 6.32 and Table 6.10 summarize the four NMOS inverter designs discussed in Secs. 6.6 to 6.9. The gate with the resistive load takes up too much area to be implemented in IC form. The saturated load configuration is the simplest circuit, using only NMOS transistors. However, it has a disadvantage in that the high logic state no longer reaches the power supply. Also, in Sec. 6.14, the speed of the saturated load gate will be demonstrated to be poorer than that of other circuit implementations. The linear load circuit solves the logic level and speed problems but requires an additional costly power supply voltage that causes wiring congestion problems in IC designs. Also note the poor value of NM_L.

Following successful development of the ion-implantation process and invention of depletion-mode load technology, NMOS circuits with depletion-mode load devices quickly became the circuit of choice. From Fig. 6.32 and Table 6.10, we see that the additional process complexity

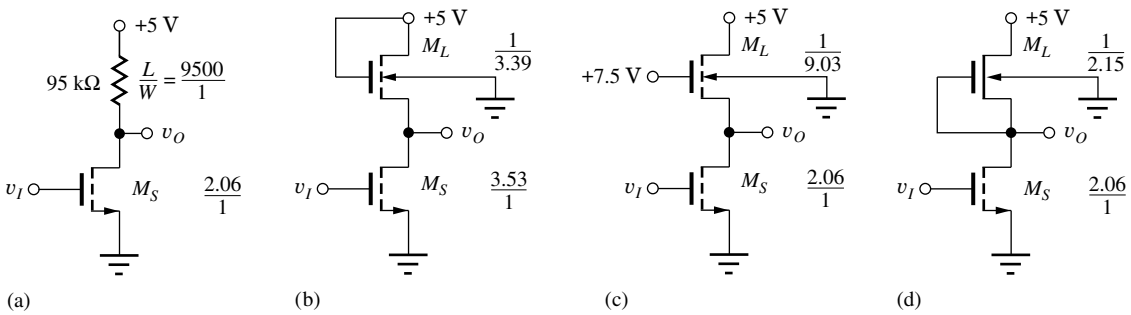


Figure 6.32 Comparison of various NMOS inverter designs: (a) Inverter with resistor load, (b) saturated load inverter, (c) linear load inverter, (d) inverter with depletion-mode load.

TABLE 6.10
Inverter Characteristics

	INVERTER WITH RESISTOR LOAD	SATURATED LOAD INVERTER	LINEAR LOAD INVERTER	INVERTER WITH DEPLETION-MODE LOAD
V_H	5.0 V	3.4 V	5.0 V	5.0 V
V_L	0.25 V	0.25 V	0.25 V	0.25 V
N_{ML}	0.34 V	0.32 V	0.02 V	0.69 V
N_{MH}	1.43 V	0.69 V	2.78 V	2.25 V
Area (μm^2)	9500	6.92	9.36	4.21

is traded for a simple inverter topology that gives $V_H = V_{DD}$ with the smallest overall transistor sizes. At the same time, the depletion-load gate yields the best combination of noise margins. At the end of the chapter, we will find that the depletion load gate also yields the highest speed of the four circuit configurations. The depletion-mode load in Sec. 6.14 tends to act as a current source during most of the output transition, and it will be found that depletion-mode logic is therefore the fastest of the four inverter configurations. We will refer to the gate designs of Fig. 6.32 as our **reference inverter designs** and use these circuits as the basis for more complex designs in subsequent sections.

Because of its many advantages, depletion-mode NMOS logic was the dominant technology for many years in the design of microprocessors. However, the large static power dissipation inherent in NMOS logic eventually limited further increases in IC chip density, and a rapid shift took place to the more complex CMOS technology, which is discussed in detail in the next chapter.

6.11 NMOS NAND AND NOR GATES

A complete logic family must provide not only the logical inversion function but also the ability to form some combination of at least two input variables such as the AND or OR function. In NMOS logic, an additional transistor can be added to the simple inverter to form either a NOR or a NAND logic gate. The NOR gate represents the combination of an OR operation followed by inversion, and the NAND function represents the AND operation followed by inversion. One of the advantages of MOS logic is the ease with which both the NOR and NAND functions can be implemented. The switching devices inherently provide the inversion operation, whereas series and parallel combinations of transistors produce the AND and OR operations, respectively.

In the following discussion, remember that we use the positive logic convention to relate voltage levels to logic variables: a high logic level corresponds to a logical 1 and a low logic level corresponds to a logical 0:

$$V_H \equiv 1 \qquad \text{and} \qquad V_L \equiv 0$$

6.11.1 NOR Gates

In Fig. 6.33, switching transistor M_S of the inverter has been replaced with two devices, M_A and M_B, to form a two-input NOR gate. If either, or both, of the inputs A and B is in the high logic state, a current path will exist through at least one of the two switching devices, and the output will be in the low logic state. Only if inputs A and B are both in the low state will the output of

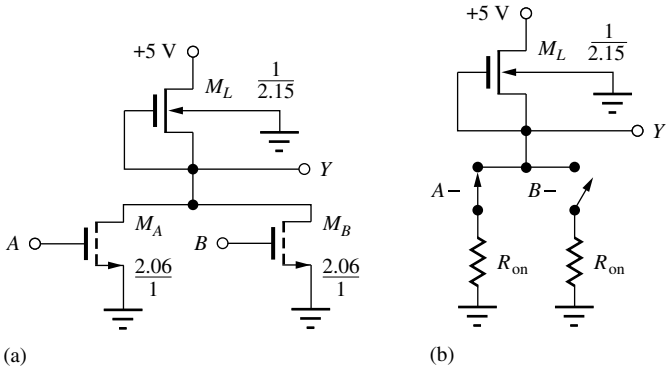


Figure 6.33 (a) Two-input NMOS NOR gate: $Y = \overline{A + B}$. (b) Simplified model with switching transistor A on.

TABLE 6.11
NOR Gate Truth Table

A	*B*	$Y = \overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0

the gate be in the high logic state. The truth table for this gate, Table 6.11, corresponds to that of the NOR function $Y = \overline{A + B}$.

We will pick the size of the devices in our logic gates based on the reference inverter design defined at the end of Sec. 6.9 [Fig. 6.32(d)]. The size of the various transistors must be chosen to ensure that the gate meets the desired logic level and power specifications under the worst-case set of logic inputs.

Consider the simplified schematic for the two-input NOR gate in Fig. 6.33(b). The worst-case condition for the output low state occurs when either M_A or M_B is conducting alone, so the on-resistance R_{on} of each individual transistor must be chosen to give the desired low output level. Thus, $(W/L)_A$ and $(W/L)_B$ should each be equal to the size of M_S in the reference inverter (2.06/1). If M_A and M_B both happen to be conducting ($A = 1$ and $B = 1$), then the combined on-resistance will be equivalent to $R_{on}/2$, and the actual output voltage will be somewhat lower than the original design value of $V_L = 0.25$ V.

When either M_A or M_B is conducting alone, the current is limited by the load device, and the voltages are exactly the same as in the reference inverter.[5] Thus, the W/L ratio of the load device is the same as in the reference inverter (1/2.15). The completed NOR gate design is given in Fig. 6.32(a).

EXERCISE: Draw the schematic of a three-input NOR gate. What are the W/L ratios for the transistors based on Fig. 6.33?

ANSWERS: 1/2.15; 2.06/1; 2.06/1; 2.06/1

6.11.2 NAND GATES

In Fig. 6.34(a), a second NMOS transistor has been added in series with the original switching device of the basic inverter to form a two-input NAND gate. Now, if inputs A and B are *both* in a high logic state, a current path exists through the series combination of the two switching devices, and the output is in a low logic state. If either input A or input B is in the low state, then

[5] Actually, the worst-case situation for current in the load device occurs when M_A and M_B are both on because the voltage is slightly higher across the load device, and its value of V_{SB} is smaller. However, this effect is small enough to be neglected. See Prob. 6.87.

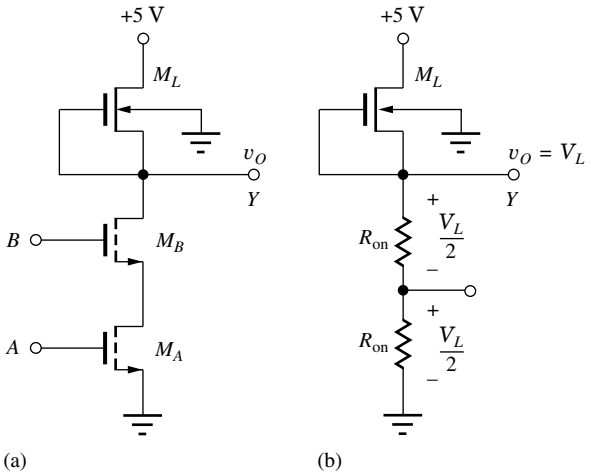


Figure 6.34 Two-input NMOS NAND gate: $Y = \overline{AB}$.

TABLE 6.12
NAND Gate Truth Table

A	B	$Y = \overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

the conducting path is broken and the output of the gate is in the high state. The truth table for this gate, Table 6.12, corresponds to that of the NAND function $Y = \overline{AB}$.

Selecting the Sizes of the Switching Transistors

The sizes of the devices in the NAND logic gate are again chosen based on the reference inverter design from Fig. 6.32(d). The W/L ratios of the various transistors must be selected to ensure that the gate still meets the desired logic level and power specifications under the worst-case set of logic inputs. Consider the simplified schematic for the two-input NAND gate in Fig. 6.34(b). The output low state occurs when both M_A and M_B are conducting. The combined on-resistance will now be equivalent to $2R_{\text{on}}$, where R_{on} is the on-resistance of each individual transistor conducting alone. In order to achieve the desired low level, $(W/L)_A$ and $(W/L)_B$ must both be approximately twice as large as the W/L ratio of M_S in the reference inverter because the on-resistance of each device in the triode region is inversely proportional to the W/L ratio of the transistor:

$$R_{\text{on}} = \frac{v_{DS}}{i_D} = \frac{1}{K_n' \dfrac{W}{L}\left(v_{GS} - V_{TN} - \dfrac{v_{DS}}{2}\right)} \tag{6.34}$$

A second way to approach the choice of device sizes is to look at the voltage across the two switching devices when v_O is in the low state. For our design, $V_L = 0.25$ V. If we assume that one-half of this voltage is dropped across each of the switching transistors and that $(v_{GS} - V_{TN}) \gg v_{DS}/2$, then it can be seen from

$$i_D = K_n'\left(\frac{W}{L}\right)_S (v_{GS} - V_{TN} - 0.5v_{DS})v_{DS} \cong K_n'\left(\frac{W}{L}\right)_S (v_{GS} - V_{TN})v_{DS} \tag{6.35}$$

that the W/L of the transistors must be approximately doubled in order to keep the current at the same value. Figure 6.35(a) shows the NAND gate design based on these arguments.

Two approximations have crept into this analysis. First, the source-bulk voltages of the two transistors are not equal, and therefore the values of the threshold voltages are slightly different for M_A and M_B. Second, $V_{GSA} \neq V_{GSB}$. From Fig. 6.35(a), $V_{GSA} = 5$ V, but $V_{GSB} = 4.875$ V. The results of taking these two effects into account are shown in Fig. 6.35(b). (Verification of

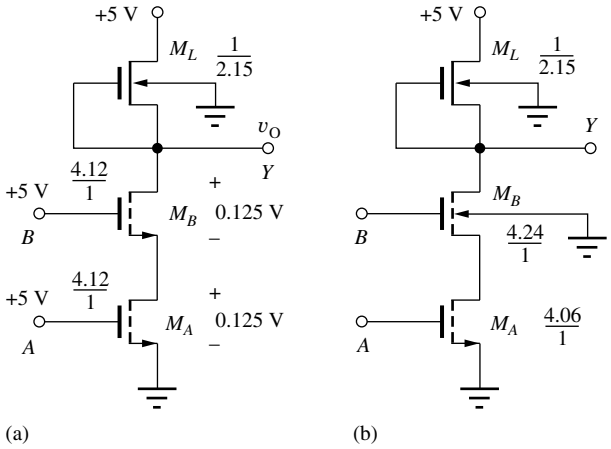


Figure 6.35 NMOS NAND gate: $Y = \overline{AB}$: (a) approximate design, (b) corrected design.

these W/L values is left for Prob. 6.88.) The corrected device sizes have changed by only a small amount. The values in Fig. 6.35(a) represent an adequate level of design for most purposes.

Choosing the Size of the Load Device

When both M_A and M_B are conducting, the current is limited by the load device, but the voltages applied to the load device are exactly the same as those in the reference inverter design. Thus, the W/L ratio of the load device is the same as in the reference inverter. The completed NAND gate design, based on the simplified device sizing, is given in Fig. 6.35(a).

EXERCISE: Draw the schematic of a three-input NAND gate. What are the W/L ratios for the transistors based on Fig. 6.35(a).

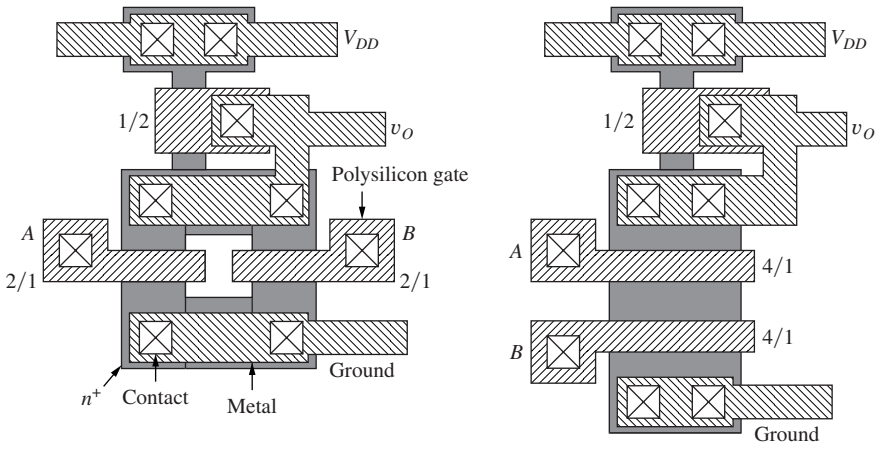
ANSWERS: 1/2.15; 6.18/1; 6.18/1; 6.18/1

6.11.3 NOR AND NAND GATE LAYOUTS IN NMOS DEPLETION-MODE TECHNOLOGY

Sample layouts for two-input NOR and two-input NAND gates appear in Fig. 6.36 based on ground rules similar to those discussed in Chapter 4. The metal overlap has been reduced in the layout to make the figure clearer.

The NOR gate has the sources and drains of switching transistors A and B connected in parallel using the n^+ layer. The source of the load device is also connected to the common drain region of the switching transistors using the n^+ layer. The gate of the load device is connected to the switching transistors using the metal layer, which also is the output terminal.

Input transistors A and B are stacked above each other in the NAND gate layout. Note that the source of transistor A and the drain of transistor B are the same n^+ region; no contacts are required between the transistors. The widths of transistors A and B have been made twice as wide to maintain the desired low output level, whereas the size of the load transistor remains unchanged.



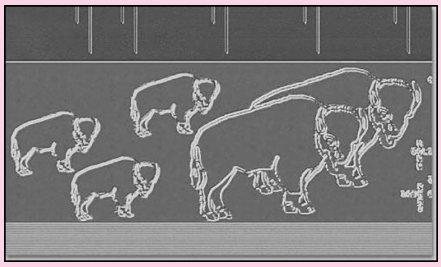
(a) Two-input NOR (b) Two-input NAND

Figure 6.36 Possible layouts for (a) two-input NOR gate and (b) two-input NAND gate.

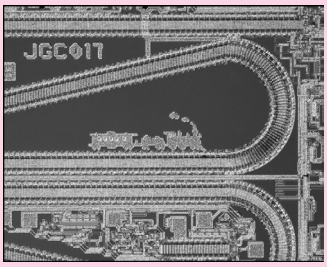
ELECTRONICS IN ACTION

Silicon Art

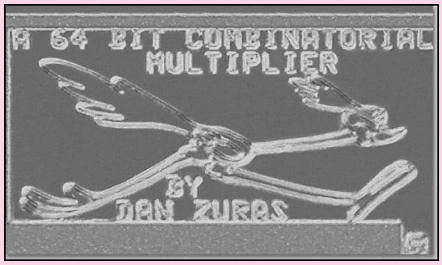
Successful integrated circuit designers are typically a very creative group of people. In the course of a large chip design project, engineers generate numerous innovations. The process involves many long hours leading up to the release of the chip layout data to manufacturing.



A small herd of buffalo added to a Hewlett-Packard 64-bit combinatorial divider created by HP engineer Dick Vlach.



A train found on an analog shift register from a LeCroy MVV200 integrated circuit.



A roadrunner drawn in aluminum on silicon by Dan Zuras of Hewlett-Packard.

A compass placed on a prototype optical navigation chip by Hewlett-Packard Labs designer Travis Blalock.

As the end of the design process nears, exhausted designers often want to add a more personal imprint on their work. Traditionally this has taken the form of using patterns in the metal layers of the chip layout to create graphical images relating to the chip's internal code name.

Sadly, most modern IC foundries are now forbidding designers to express themselves in this way over concerns about design rule violations and potential processing problems. Designers tell us that this has forced them to become covert with their doodles and they are sometimes embedding the graphics directly into functional design structures.

6.12 COMPLEX NMOS LOGIC DESIGN

A major advantage of MOS logic over various forms of bipolar logic comes through the ability to directly combine NAND and NOR gates into more complex configurations. Three examples of **complex logic gate** design are discussed in this section.

Consider the circuit in Fig. 6.37. The output Y will be in a low state whenever a conducting path is developed through the switching transistor network. For this circuit, the output voltage will be low if any one of the following paths is conducting: A or BC (B and C) or BD (B and D). The output Y is represented logically as

$$\overline{Y} = A + BC + BD \quad \text{or} \quad Y = \overline{A + BC + BD} \quad \text{or} \quad Y = \overline{A + B(C + D)}$$

which directly implements a complemented **sum-of-products logic function.**

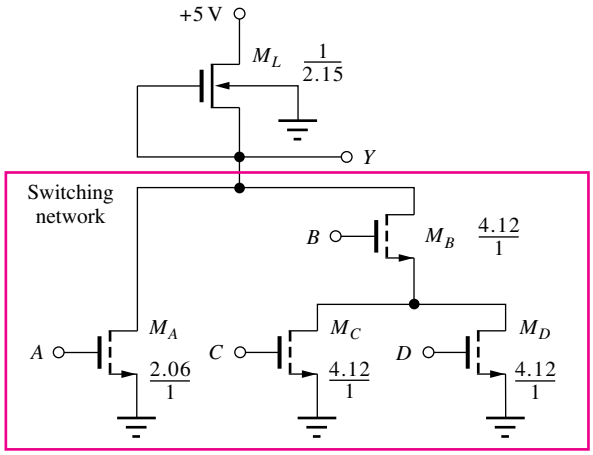


Figure 6.37 Complex NMOS logic gate: $Y = \overline{A + BC + BD}$.

Device sizing will again be based on the worst-case logic state situations. Referring to the reference inverter design, device M_A must have $W/L = 2.06/1$ because it must be able to maintain the output at 0.25 V when it is the only device that is conducting. In the other two paths, M_B will appear in series with either M_C or M_D. Thus, in the worst case, there will be two devices in series in this path, and the simplest choice will be $M_B = M_C = M_D = 4.12/1$. The load device size remains unchanged.

The circuit in Fig. 6.38 provides a second example of transistor sizing in complex logic gates. There are two possible conducting paths through the switching transistor network: AB (A and B)

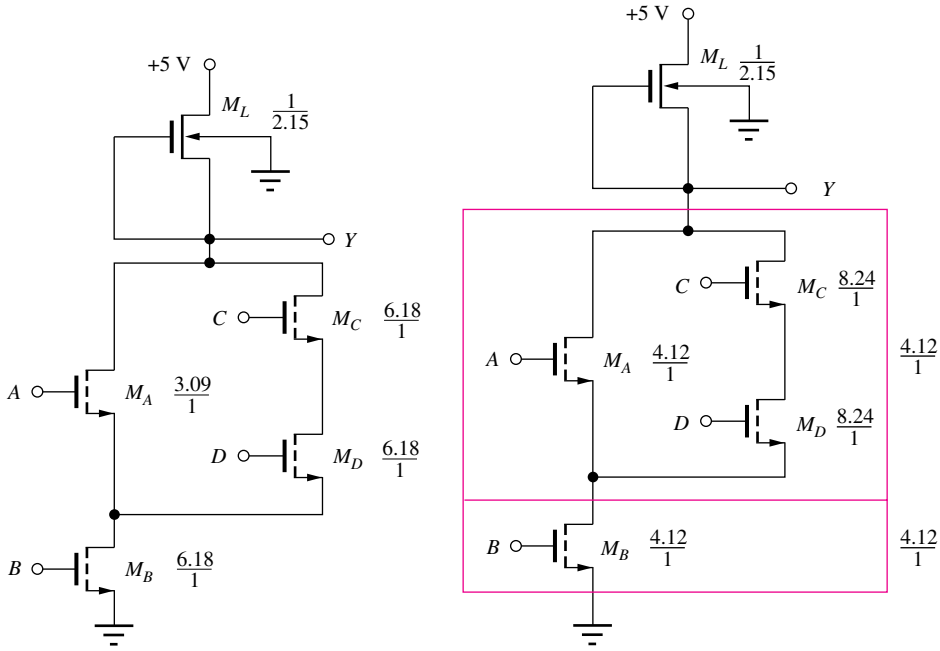


Figure 6.38 (a) NMOS implementation of $Y = \overline{AB + CDB}$ or $Y = \overline{(A + CD)B}$. (b) An alternate transistor sizing for the logic gate in (a).

or CDB (C and D and B). The output will be low if either path is conducting, resulting in

$$\overline{Y} = AB + CDB \qquad \text{or} \qquad Y = \overline{AB + CDB} \qquad \text{or} \qquad Y = \overline{(A + CD)B}$$

Transistor sizing can be done in two ways. In the first method, we find the worst-case path in terms of transistor count. For this example, path CDB has three transistors. By making each transistor three times the size of the reference switching transistor, the CDB path will have an on-resistance equivalent to that of M_S in the reference inverter. Thus, each of the three transistors should have $W/L = 6.18/1$.

The second path contains transistors M_A and M_B. In this path, we want the sum of the on-resistances of the devices to be equal to the on-resistance of M_S in the reference inverter:

$$\frac{R_{\text{on}}}{\left(\frac{W}{L}\right)_A} + \frac{R_{\text{on}}}{\left(\frac{W}{L}\right)_B} = \frac{R_{\text{on}}}{\left(\frac{W}{L}\right)_S} \tag{6.36}$$

In Eq. (6.36), R_{on} represents the on-resistance of a transistor with $W/L = 1/1$. Because $(W/L)_B$ has already been chosen,

$$\frac{R_{\text{on}}}{\left(\frac{W}{L}\right)_A} + \frac{R_{\text{on}}}{6.18} = \frac{R_{\text{on}}}{2.06} \tag{6.37}$$

Solving for $(W/L)_A$ yields a value of $3.09/1$. Because the operating current of the gate is to be the same as the reference inverter, the geometry of the load device remains unchanged. The completed design values appear in Fig. 6.38(a).

A slightly different approach is used to determine the transistor sizes for the same logic gate in Fig. 6.38(b). The switching circuit can be partitioned into two sub-networks connected in series: transistor B in series with the parallel combination of A and CD. We make the equivalent on-resistance of these two subnetworks equal. Because the two subnetworks are in series, $(W/L)_B = 2(2.06/1) = 4.12/1$. Next, the on-resistance of each path through the $(A + CD)$ network should also be equivalent to that of a $4.12/1$ device. Thus $(W/L)_A = 4.12/1$ and $(W/L)_C = (W/L)_D = 8.24/1$. These results appear in Fig. 6.38(b).

6.12.1 Selecting Between the Two Designs

If the unity dimension corresponds to the minimum feature size F, then the total gate area of the switching transistors for the design in Fig. 6.38(b) is $24.7F^2$. The previous implementation of Fig. 6.38(a) had a total gate area of $21.6F^2$. With this yardstick, the second design requires 14 percent more area than the first. Minimum area utilization is often a key consideration in IC design, and the device sizes in Fig. 6.38(a) would be preferred over those in Fig. 6.38(b).

DESIGN EXAMPLE 6.10 **TRANSISTOR SIZING IN COMPLEX LOGIC GATES**

Choose the transistor sizes for a complex logic gate based on a given reference inverter design.

PROBLEM Find the logic expression for the gate in Fig. 6.39. Design the W/L ratios of the transistors based on the reference inverter in Fig. 6.32(d).

SOLUTION **Known Information and Given Data:** Logic circuit diagram in Fig. 6.39; reference inverter design in Fig. 6.32(d) with $(W/L)_S = 2.06/1$ and $(W/L)_L = 1/2.15$.

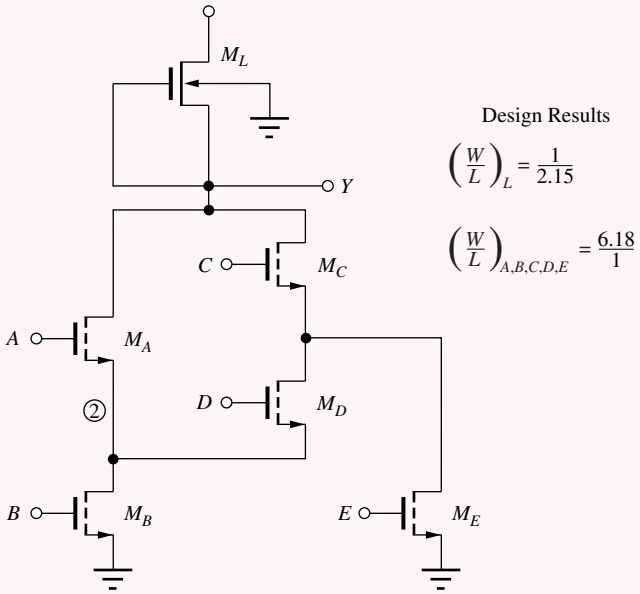


Figure 6.39 NMOS implementation of $Y = \overline{AB + CDB + CE + ADE}$.

Unknowns: Logic expression for output Y; W/L ratios for all the transistors

Approach: Identify the conducting paths that force the output low; output Y can be represented as a complemented sum-of-products function of the conducting path descriptions. Size the transistors in each path to yield the same on-resistance as the reference inverter.

Assumptions: Neglect the effects of the small source-bulk voltages on the switching transistors. Neglect V_{GS} differences among the switching transistors.

Analysis: Comparing the circuit in Fig. 6.39 to that in 6.38, we see that a fifth transistor has been added to the switching network. Now there are *four* possible conducting paths through the switching transistor network: AB or CDB or CE or ADE. The output will be low when any one of these paths is conducting, resulting in

$$\overline{Y} = AB + CDB + CE + ADE \qquad \text{or} \qquad Y = \overline{AB + CDB + CE + ADE}$$

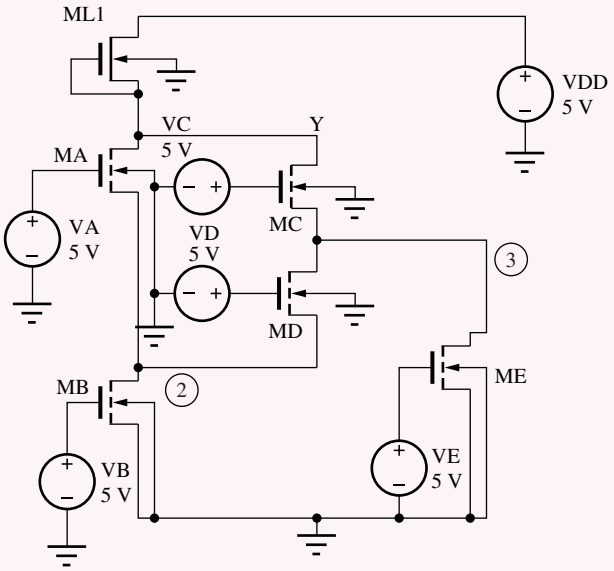
We desire the current and power to be the same in the circuit when the output is in the low state. Thus the load device will be identical to that of the inverter. The switching transistor network cannot be broken into series and parallel branches, and transistor sizing will follow the worst-case path approach. Path CDB has three transistors in series, so each W/L will be set to three times that of the switching transistor in the reference inverter, or 6.18/1. Path ADE also has three transistors in series, and, because D has $(W/L) = 6.18/1$, the W/L ratios of A and E can also be 6.18/1. All transistors are now 6.18/1 devices.

Check of Results: The remaining paths, AB and CE, must be checked to ensure that the low output level will be properly maintained. Each has two transistors with $W/L = 6.18/1$ in series for an equivalent $W/L = 3.09/1$. Because the W/L of 3.09/1 is greater than 2.06/1, the low output state will be maintained at $V_L < 0.25$ V when paths AB or CE are conducting.

Discussion: Note that the current traverses transistor D in one direction when path CDB is conducting, but in the opposite direction when path ADE is active! Remember from the device cross section in Fig. 6.32(b) that the MOS transistor is a symmetrical device. The only way to actually tell the drain terminal from the source terminal is from the values of the applied potentials. For the NMOS transistor, the drain terminal will be the terminal at the higher voltage, and the source terminal will be the terminal at the lower potential. This bidirectional nature of the MOS transistor is a key to the design of high-density dynamic random access memories (DRAMs), which are discussed in Chapter 8.

Computer-Aided Design: Now we can use SPICE to find the actual values of V_L for different input combinations including the influence of body effect and nonzero source voltages on the operation of the gate. For the circuit below with VTO = 0.75, KP = 25E-6, GAMMA = 0.5, PHI = 0.6, W = 6.18 U, and L = 1 U for the switching devices and VTO = −3, KP = 25E-6, GAMMA = 0.5, PHI = 0.6, W = 1 U, and L = 2.15 U for the load device, SPICE gives these results:

ABCDE	*Y* (mV)	Node 2 (mV)	Node 3 (mV)	I_{DD} (μA)
11000	158	77.9	0	50.7
01110	236	155	76.7	49.9
00101	158	0	77.9	50.7
11111	79.2	39.4	39.4	51.5



EXERCISE: (a) Calculate the power supply current I_{DD} if the voltage at node Y is 158 mV. (b) Repeat for 79.2 mV. (c) Repeat for 236 mV.

ANSWERS: (a) 50.7 μA; (b) 51.5 μA; (c) 49.9 μA

EXERCISE: Make a complete table for node voltages Y, 2, and 3 and I_{DD} for all 32 possible combinations of inputs for the circuit in Ex. 6.10. Fill in the table entries based on the SPICE simulation results presented in the example.

6.13 POWER DISSIPATION

In this section we consider the two primary contributions to power dissipation in NMOS inverters. The first is the steady-state power dissipation that occurs when the logic gate output is stable in either the high or low states. The second is power that is dissipated in order to charge and discharge the total equivalent load capacitance during dynamic switching of the logic gate.

6.13.1 STATIC POWER DISSIPATION

The overall **static power dissipation** of a logic gate is the average of the power dissipations of the gate when its output is in the low state and the high state. The power supplied to the logic gate is expressed as $P = V_{DD} i_{DD}$, where i_{DD} is the current provided by the source V_{DD}. In the circuits considered so far, i_{DD} is equal to the current through the load device, and the total power supplied by source V_{DD} is dissipated in the load and switching transistors. The average power dissipation depends on the fraction of time that the output spends in the two logic states. If we assume that the average logic gate spends one-half of the time in each of the two output states (a 50 percent

duty cycle), then the average power dissipation is given by

$$P_{\text{av}} = \frac{V_{DD}I_{DDH} + V_{DD}I_{DDL}}{2} \tag{6.38}$$

where I_{DDH} = current in gate for $v_O = V_H$
I_{DDL} = current for $v_O = V_L$

For the NMOS logic gates considered in this chapter, the current in the gate becomes zero when the v_O reaches V_H. Thus, $I_{DDH} = 0$, and the average power dissipation becomes equal to one-half the power dissipation when the output is low, given by

$$P_{\text{av}} = \frac{V_{DD}I_{DDL}}{2} \tag{6.39}$$

If some other duty factor is deemed more appropriate (for example, 33 percent), it simply changes the factor of 2 in the denominator of Eq. (6.39).

EXERCISE: What is the average power dissipation of the gates in Fig. 6.32?

ANSWER: 0.125 mW

6.13.2 DYNAMIC POWER DISSIPATION

A second, very important source of power dissipation is **dynamic power dissipation,** which occurs during the process of charging and discharging the load capacitance of a logic gate. Consider the simple circuit in Fig. 6.40(a), in which a capacitor is being charged toward the positive voltage V_{DD} through a nonlinear resistor (such as a MOS load device).

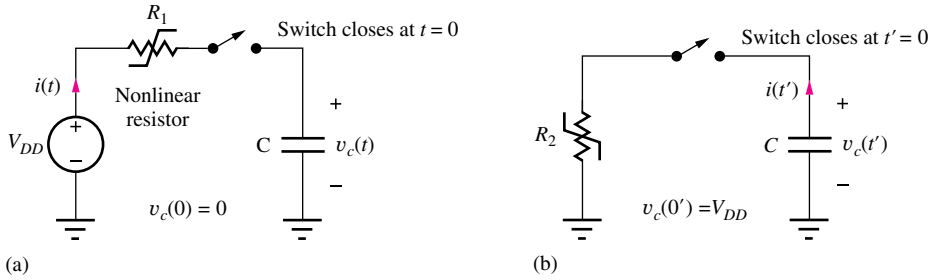


Figure 6.40 Simple circuit model for dynamic power calculation: (a) charging C, (b) discharging C.

Let us assume the capacitor is initially discharged; at $t = 0$ the switch closes, and the capacitor then charges toward its final value. We also assume that the nonlinear element continues to deliver current until the voltage across it reaches zero (for example, a depletion-mode load). The total energy E_D delivered by the source is given by

$$E_D = \int_0^\infty P(t)\,dt \tag{6.40}$$

The power $P(t) = V_{DD}i(t)$, and because V_{DD} is a constant,

$$E_D = V_{DD}\int_0^\infty i(t)\,dt \tag{6.41}$$

The current supplied by source V_{DD} is also equal to the current in capacitor C, and so

$$E_D = V_{DD} \int_0^{\infty} C \frac{dv_C}{dt} dt = CV_{DD} \int_{V_C(0)}^{V_C(\infty)} dv_C \tag{6.42}$$

Integrating from $t = 0$ to $t = \infty$, with $V_C(0) = 0$ and $V_C(\infty) = V_{DD}$ results in

$$E_D = CV_{DD}^2 \tag{6.43}$$

We also know that the energy E_S stored in capacitor C is given by

$$E_S = \frac{CV_{DD}^2}{2} \tag{6.44}$$

and thus the energy E_L lost in the resistive element must be

$$E_L = E_D - E_S = \frac{CV_{DD}^2}{2} \tag{6.45}$$

Now consider the circuit in Fig. 6.40(b), in which the capacitor is initially charged to V_{DD}. At $t' = 0$, the switch closes and the capacitor discharges toward zero through another nonlinear resistor (such as an enhancement-mode MOS transistor). Again, we wait until the capacitor reaches its final value, $V_C = 0$. The energy E_S that was stored on the capacitor has now been completely dissipated in the resistor. The total energy E_{TD} dissipated in the process of first charging and then discharging the capacitor is equal to

$$E_{TD} = \frac{CV_{DD}^2}{2} + \frac{CV_{DD}^2}{2} = CV_{DD}^2 \tag{6.46}$$

Thus, every time a logic gate goes through a complete switching cycle, the transistors within the gate dissipate an energy equal to E_{TD}. Logic gates normally switch states at some relatively high frequency f (switching events/second), and the dynamic power P_D dissipated by the logic gate is then

$$P_D = CV_{DD}^2 f \tag{6.47}$$

In effect, an average current equal to $(CV_{DD}f)$ is supplied from the source V_{DD}.

EXERCISE: **What is the dynamic power dissipated by alternately charging and discharging a 1-pF capacitor between 5 V and 0 V at a frequency of 10 MHz?**

ANSWER: **0.25 mW**

Note that the power dissipation in the previous exercise is the same as the static power dissipation that we allocated to the $v_O = V_{OL}$ state in our original NMOS logic gate design. In high-speed logic systems, the dynamic component of power can become dominant — we see in the next chapter that this is in fact the primary source of power dissipation in CMOS logic gates!

6.13.3 Power Scaling in MOS Logic Gates

During logic design in complex systems, gates with various power dissipations are often needed to provide different levels of drive capability and to drive different values of load capacitance at different speeds. For example, consider the saturated load inverter in Fig. 6.41(a). The static power dissipation is determined when $v_O = V_L$. M_S is operating in the linear region, M_L is saturated, and the drain currents of the two transistors are given by

$$i_{DL} = \frac{K_n'}{2}\left(\frac{W}{L}\right)_L (v_{GSL} - V_{TNL})^2$$
$$i_{DS} = K_n'\left(\frac{W}{L}\right)_S \left(v_{GSS} - V_{TNS} - \frac{v_{DSS}}{2}\right) v_{DSS} \tag{6.48}$$

in which the W/L ratios have been chosen so that $i_{DS} = i_{DL}$ for $v_O = V_L$. For fixed voltages, both drain currents are directly proportional to their respective W/L ratios. If we double the W/L ratio of the load device *and* the switching device, then the drain currents both double, with no change in operating voltage levels.

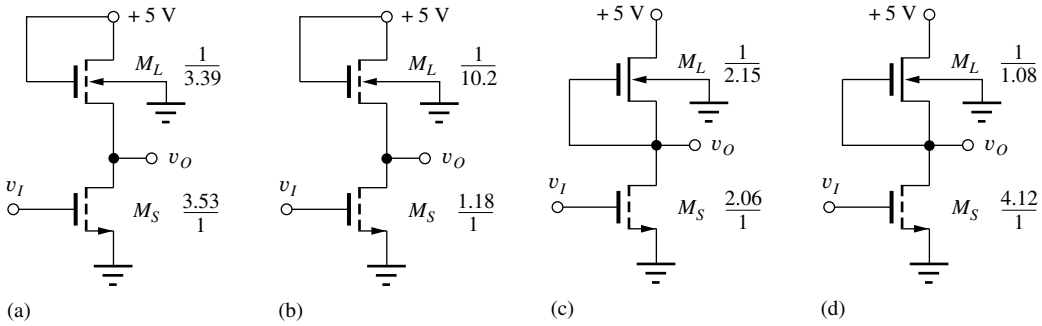


Figure 6.41 Inverter power scaling. The NMOS inverter of (b) operates at one-third the power of circuit (a), and the NMOS inverter of (d) operates at twice the power of circuit (c).

Or, if we reduce the W/L ratios of both the load device and the switching device by a factor of 3, then the drain currents are both reduced by a factor of 3, with no change in operating voltage levels. Thus, if the W/L ratios of M_L and M_S are changed by the same factor, the power level of the gate can easily be scaled up and down without affecting the values of V_H and V_L. With this technique, the inverter in Fig. 6.41(b) has been designed to operate at one-third the power of the inverter of Fig. 6.41(a) by reducing the value of W/L of each device by a factor of 3. This **power scaling** is a property of ratioed logic circuits. The power level can be scaled up or down without disturbing the voltage levels of the design.

Similar arguments can be used to scale the power levels of any of the NMOS gate configurations that we have studied, and the depletion-mode load inverter in Fig. 6.41(d) has been designed to operate at twice the power of the inverter of that of Fig. 6.41(c) by increasing the value of W/L of each device by a factor of 2. As we will see shortly, this same technique can also be used to scale the dynamic response time of the inverter to compensate for various capacitive load conditions.

Exercise: What are the new W/L ratios for the transistors in the gate in Fig. 6.41(a) for a power of 0.1 mW?

Answers: 1/8.48 and 1.41/1

EXERCISE: What are the new W/L ratios for the transistors in the gate in Fig. 6.41(c) for a power of 10 mW?

ANSWERS: 18.6/1 and 82.4/1

EXERCISE: What are the W/L ratios of the transistors in the gate in Fig. 6.38(a) required to reduce the power by a factor of three while maintaining the same value of V_L?

ANSWERS: 1/6.45; 1.03/1; 2.06/1; 2.06/1; 2.06/1

6.14 DYNAMIC BEHAVIOR OF MOS LOGIC GATES

Thus far in this chapter the discussion has been concerned with only the static design of NMOS logic gates. The time domain response, however, plays an extremely important role in the application of logic circuits. There are delays between input changes and output transitions in logic circuits because every node is shunted by capacitance to ground and is not able to change voltage instantaneously. This section reviews the sources of capacitance in the MOS circuit and then explores the dynamic or time-varying behavior of logic gates. Calculations of rise time t_r, fall time t_f, and the average propagation delay τ_p (all defined in Sec. 6.3) are presented, and expressions are then developed for estimating the response time of various inverter configurations.

6.14.1 CAPACITANCES IN LOGIC CIRCUITS

Figure 6.42(a) shows two NMOS inverters including the various capacitances associated with each transistor. These capacitances were introduced in Sec. 4.6. Each device has capacitances between its gate-source, gate-drain, source-bulk, and drain-bulk terminals. Some of the capacitances do not appear in the schematic because they are shorted out by the various circuit connections (for example, C_{SB1}, C_{GS2}, C_{SB3}, C_{GS4}). In addition to the **MOS device capacitances,** the figure includes a wiring capacitance C_W, representing the capacitance of the electrical interconnection between the two logic gates. For simplicity in analyzing the delay times in logic circuits, the capacitances on a given node will be lumped together into a fixed effective nodal capacitance C, as indicated in Fig. 6.42(b), and our hand analysis will cast the behavior of circuits in terms of this effective capacitance C. The MOS device capacitances are nonlinear functions of the various node voltages; they are highly dependent on circuit layout in an integrated circuit. We will not attempt to find a precise expression for C in terms of all the capacitances in Fig. 6.42(a), but we assume that we have an estimate for the value of C. Simulation tools exist that will extract values of C from a given IC layout, and more accurate predictions of time-domain behavior can be obtained using SPICE circuit simulations.

Fan-Out Limitations in NMOS Logic

Since no dc current needs to be supplied to the input of an NMOS logic gate, the fan-out of an MOS logic gate is not limited by static design constraints. (But, this is not the case for bipolar design discussed later in Chapter 9.) However, as more and more gates are attached to a given output as in Figs. 6.42 or 6.14, the value of capacitor C increases, and as we shall see shortly, the temporal responses of the circuit will decrease accordingly. Thus the fan-out will be limited by how much degradation can be tolerated in the time delays of the circuit.

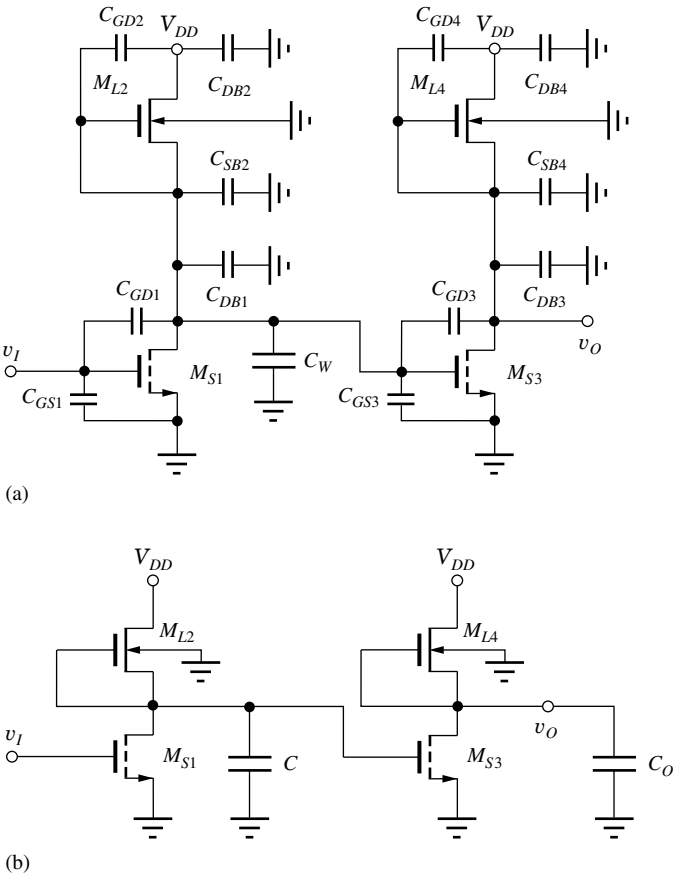


Figure 6.42 (a) Capacitances associated with an inverter pair. (b) Lumped-load capacitance model for inverters.

6.14.2 Dynamic Response of the NMOS Inverter with a Resistive Load

Figure 6.43 shows the circuit from our earlier discussion of the inverter with a resistive load. For hand analysis, the logic input signal is represented by an ideal step function, and we now calculate the rise time, fall time, and delay times for this inverter.

Calculation of t_r and τ_{PLH}

For analysis of the rise time, assume that the input and output voltages have reached their steady-state levels for $t < 0$: $v_I = V_H = 5$ V and $v_O = V_L = 0.25$ V. At $t = 0$, the input drops from $v_I = 5$ V to $v_I = 0.25$ V. Because the gate-source voltage of the switching transistor drops below V_{TNS}, the MOS transistor abruptly stops conducting. The output then charges from $v_O = V_L = 0.25$ V to $v_O = V_H = V_{DD} = 5$ V. In this case, the waveform is that of the simple RC network formed by the load resistor R and the load capacitor C. Using our knowledge of single-time constant circuits:

$$v_O(t) = V_F - (V_F - V_I)\exp\left(-\frac{t}{RC}\right) = V_F - \Delta V \exp\left(-\frac{t}{RC}\right) \tag{6.49}$$

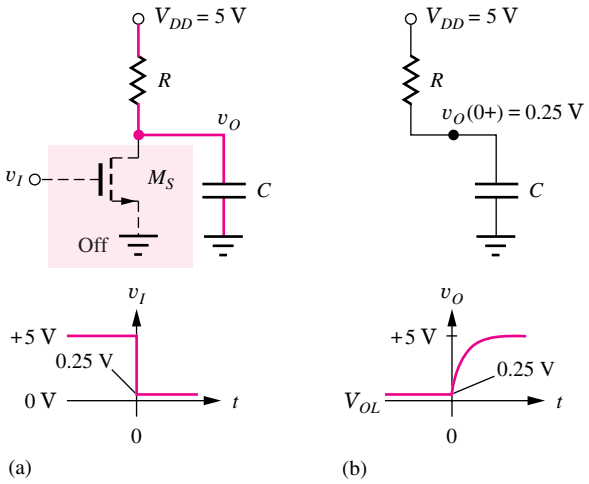


Figure 6.43 Model for rise time in resistively loaded inverter.

where V_F is the final value of the capacitor voltage, V_I is the initial capacitor voltage, and $\Delta V = (V_F - V_I)$ is the change in the capacitor voltage. For the inverter in Fig. 6.43, $V_F = 5.0$ V, $V_I = 0.25$ V, and $\Delta V = 4.75$ V.

The rise time is determined by the difference between the time t_1 when $v_O(t_1) = V_I + 0.1\,\Delta V$ and the time t_2 when $v_O(t_2) = V_I + 0.9\,\Delta V$. Using Eq. (6.49),

$$V_I + 0.1\,\Delta V = V_F - \Delta V \exp\left(\frac{-t_1}{RC}\right) \qquad \text{yields} \qquad t_1 = -RC \ln 0.9 \tag{6.50}$$

$$V_I + 0.9\,\Delta V = V_F - \Delta V \exp\left(\frac{-t_2}{RC}\right) \qquad \text{yields} \qquad t_2 = -RC \ln 0.1 \tag{6.51}$$

and

$$t_r = t_2 - t_1 = RC \ln 9 = 2.2RC \tag{6.52}$$

The delay time τ_{PLH} is determined by $v_O(\tau_{PLH}) = V_I + 0.5\,\Delta V$, which yields

$$\tau_{PLH} = -RC \ln 0.5 = 0.69RC \tag{6.53}$$

Note that these expressions apply only to the simple RC network.

Equations (6.52) and (6.53) represent the classical expressions for the rise time and propagation delay for an RC network. Similar analyses show that $t_f = 2.2RC$ and $t_{PHL} = 0.69RC$. Remember that these expressions only apply to the simple RC network.

DESIGN NOTE

The rise and fall times and propagation delays for an RC network are given by

$$t_r = t_f = 2.2RC \qquad t_{PLH} = t_{PHL} = 0.69RC$$

EXERCISE: Find the t_r and τ_{PLH} for the resistively loaded inverter with $C = 0.2$ pF and $R = 95$ kΩ.

ANSWERS: 41.8 ns; 13.1 ns

EXERCISE: Derive expressions for the fall time and high-to-low propagation delay for an *RC* network.

ANSWERS: $t_f = 2.2RC$; $t_{PHL} = 0.69RC$

Calculation of τ_{PHL} and t_f

Now consider the other switching situation, with $v_I = V_L = 0.25$ V and $v_O = V_H = 5$ V, as displayed in Fig. 6.44. At $t = 0$, the input abruptly changes from $v_I = 0.25$ V to $v_I = 5$ V. At $t = 0^+$, M_S has $v_{GS} = 5$ V and $v_{DS} = 5$ V, so it conducts heavily and discharges the capacitance until the value of v_O reaches V_L.

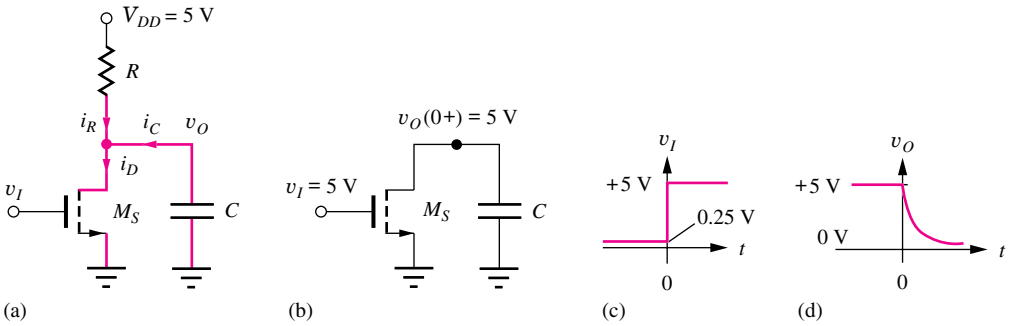


Figure 6.44 Simplified circuit for determining t_f and τ_{PHL}. $N_I(0^+) = V_H = V_{DD}$.

Figure 6.45 shows the currents i_R and i_D in the load resistor and switching transistor as a function of v_O during the transition between V_H and V_L. The current available to discharge the capacitor C is the difference in these two currents:

$$i_C = i_D - i_R$$

Because the load element is a linear resistor, the current in the resistor increases linearly as v_O goes from V_H to V_L. However, when M_S first turns on, a large drain current occurs, rapidly discharging the load capacitance C. V_L is reached when the current through the capacitor becomes zero and $i_R = i_D$. Note that the drain current is much greater than the current in the resistor for most of the period of time corresponding to τ_{PHL}. This leads to values of τ_{PHL} and t_f that are much shorter than τ_{PLH} and t_r associated with the rising output waveform. This behavior is characteristic of single channel (NMOS or PMOS) logic circuits. Another way to visualize this difference is to remember that the on-resistance of the MOS transistor must be much smaller than R in order to force V_{OL} to be a low value. Thus, the apparent "time constant" for the falling waveform will be much smaller than that of the rising waveform.

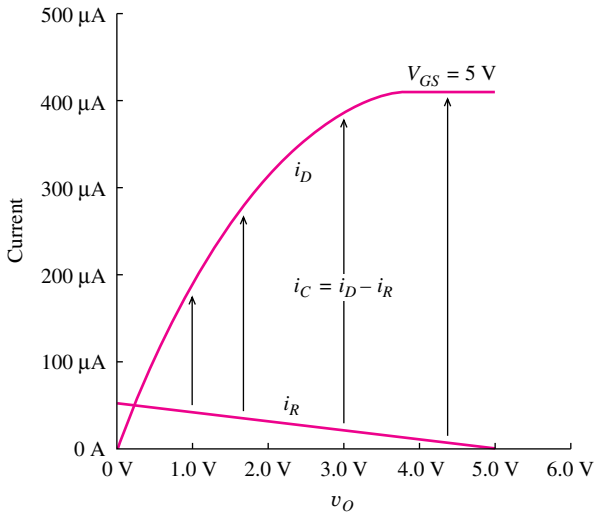


Figure 6.45 Drain current and resistor current versus v_O.

Calculation of t_f and τ_{PHL} is more complicated here than for the case of the resistor charging the capacitive load because the NMOS transistor changes regions of operation during the output voltage transition. Thus, the differential equation that models the V_H to V_L transition changes at the point at which the transistor changes operating regions.

First, let us simplify our model for the circuit. From Fig. 6.45, we can see that $i_D \gg i_R$ except for v_O very near V_L. Therefore, the current through the resistor will be neglected so that we can assume that all the drain current of the NMOS transistor is available to discharge the load capacitance, as in Fig. 6.44(b). The input signal v_I is assumed to be a step function changing to $v_I = 5$ V at $t = 0$. At $t = 0$, the output voltage V_C on the capacitor is $V_H = V_{DD} = 5$ V, and the gate voltage is forced to $V_G = 5$ V.

The graph in Fig. 6.46 shows the important instants in time that need to be considered. At time t_1 the output has dropped by 10% of the logic swing ΔV, and time t_4 is the time at which

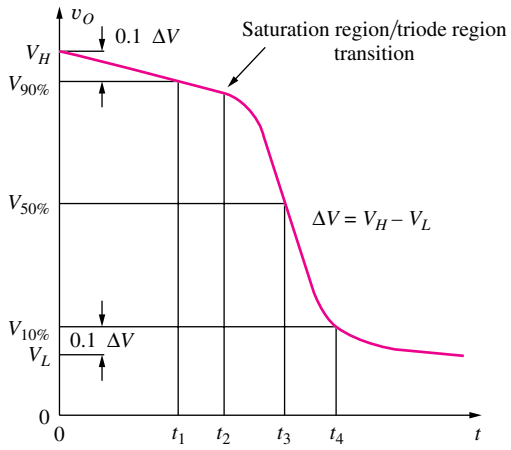


Figure 6.46 Times needed for calculation of τ_{PHL} and t_f for the inverter. Fall time $t_f = t_4 - t_1$; propagation delay $\tau_{PHL} = t_3$.

the output has dropped by 90% of ΔV. Thus, $t_f = t_4 - t_1$. At t_3, the output is at the 50% point, given by $V_{50\%} = (V_H + V_L)/2$, so $\tau_{PHL} = t_3$. Time t_2 is also very important. At this point $v_O = V_{DD} - V_{TNS}$, and this is the time at which the transistor changes from saturation region operation to triode region operation. Thus, the differential equation that models the circuit behavior changes at this point. This regional approach is used so often that it is referred to as piecewise analysis.

Piecewise Analysis of τ_{PHL}

Let us first focus on calculation of τ_{PHL} and then calculate t_f. At $t = 0^+$, the NMOS transistor in Fig. 6.44(b) is operating in the saturation region, and the capacitor current is described by

$$\frac{K_S}{2}(v_{GS} - V_{TNS})^2 = -C\frac{dv_C}{dt} \qquad \text{with } v_C(0^+) = V_H \tag{6.54}$$

in which $v_{GS} = V_H$ and V_{TNS} are both constant. Thus, the drain current is constant, and the capacitor discharges at a constant rate until the MOSFET enters the linear region of operation at time t_2, when $v_C = v_{GS} - V_{TNS}$. The MOSFET enters the linear region after the capacitor voltage drops by one threshold voltage. For these values, the time t_2 required for the transistor to reach the linear region is

$$t_2 = \frac{2CV_{TNS}}{K_S(V_H - V_{TNS})^2} = 2R_{\text{onS}}C\frac{V_{TNS}}{(V_H - V_{TNS})} \tag{6.55}$$

for

$$R_{\text{onS}} = \frac{1}{K_S(V_H - V_{TNS})}$$

which represents the equivalent on-resistance of the NMOS switching transistor, with $v_{GS} = V_{DD}$ and $v_{DS} = 0$.

Once the transistor enters the triode region, the equation characterizing the discharge changes to

$$K_S\left(v_{GS} - V_{TNS} - \frac{v_C}{2}\right)v_C = -C\frac{dv_C}{dt} \tag{6.56}$$

because the $v_{DS} = v_C$ for the MOSFET. Rearranging this equation with $v_{GS} = V_H$ and integrating yields

$$\int_{V_2}^{V_3} \frac{dv_C}{(2(V_H - V_{TNS}) - v_C)v_C} = \int_{t_2}^{t_3} \frac{K_S}{2C}\,dt \tag{6.57}$$

in which the limits of integration are

$$V_2 = v_C(t_2) = V_H - V_{TNS} \qquad \text{and} \qquad V_3 = v_C(t_3) = 0.5(V_H + V_L)$$

The solution to this equation may be found using:

$$\int \frac{dx}{(a-x)x} = \frac{1}{a}\ln\left(\frac{x-a}{x}\right) \tag{6.58}$$

Using Eq. (6.58), $t_3 - t_2$ can be found to be

$$t_3 - t_2 = \frac{C}{K_S(V_H - V_{TNS})} \ln\left\{\left(\frac{V_2}{V_3}\right)\left[\frac{V_3 - 2(V_H - V_{TNS})}{V_2 - 2(V_H - V_{TNS})}\right]\right\} \tag{6.59}$$

$$t_3 - t_2 = R_{\text{onS}} C \ln\left[4\left(\frac{V_H - V_{TNS}}{V_H + V_L}\right) - 1\right] \tag{6.60}$$

The propagation time τ_{PHL} is just equal to t_3 and is given by

$$\tau_{PHL} = t_3 = (t_3 - t_2) + t_2 = R_{\text{onS}} C \left\{\ln\left[4\left(\frac{V_H - V_{TNS}}{V_H + V_L}\right) - 1\right] + \frac{2V_{TNS}}{V_H - V_{TNS}}\right\} \tag{6.61}$$

This is an extremely useful equation. Not only does it describe the behavior of the NMOS circuit, but we will also see later that Eq. (6.61) characterizes the delay behavior of CMOS logic gates, which form today's most widely used logic family.

Piecewise Analysis of t_f

Fall time t_f can be written as:

$$t_f = t_4 - t_1 = (t_4 - t_2) - (t_2 - t_1)$$

During the time interval $t_1 - t_2$, the MOSFET is saturated, and the current discharging the capacitor is constant. Therefore, using

$$\Delta t = C\frac{\Delta V}{I}$$

$$t_2 - t_1 = C\frac{(V_H - 0.1\,\Delta V) - (V_H - V_{TNS})}{\frac{K_s}{2}(V_H - V_{TNS})^2} = 2R_{\text{onS}} C \frac{V_{TNS} - 0.1\Delta V}{V_H - V_{TNS}} \tag{6.62}$$

During the interval t_2 to t_4, the MOSFET is operating in the triode region, and the circuit is described by

$$\int_{V_2}^{V_4} \frac{dv_C}{(2(V_H - V_{TNS}) - v_C)v_C} = \int_{t_2}^{t_4} \frac{K_S}{2C}\, dt \tag{6.63}$$

based on Eqs. (6.56) and (6.57) in which the limits of integration are now defined by

$$V_2 = v_C(t_2) = V_H - V_{TNS} \qquad \text{and} \qquad V_4 = v_C(t_3) = V_H - 0.9\,\Delta V \tag{6.64}$$

Using the results from (6.58) and (6.59),

$$t_4 - t_2 = R_{\text{onS}} C \ln\left(\frac{V_H - 2V_{TNS} + 0.9\,\Delta V}{V_H - 0.9\,\Delta V}\right) \tag{6.65}$$

and our estimate for the fall time is given by

$$t_f = t_4 - t_1 = R_{\text{onS}} C \left[\ln\left(\frac{V_H - 2V_{TNS} + 0.9\,\Delta V}{V_H - 0.9\,\Delta V}\right) + 2\left(\frac{V_{TNS} - 0.1\,\Delta V}{V_H - V_{TNS}}\right)\right] \tag{6.66}$$

EXAMPLE 6.11 DYNAMIC PERFORMANCE OF THE INVERTER WITH RESISTOR LOAD

Find numerical values for the dynamic performance measures of the reference inverter in Fig. 6.32(a).

PROBLEM Find t_f, t_r, τ_{PHL}, τ_{PHL}, and τ_p for the resistively loaded inverter in Fig. 6.32 with $C = 0.1$ pF and $R = 95$ kΩ.

SOLUTION **Known Information and Given Data:** Basic resistively loaded inverter circuit in Fig. 6.32; $R = 95$ kΩ, $C = 0.1$ pF, $V_{DD} = 5$ V, $W/L = 2.06/1$, $V_H = 5$ V, $V_L = 0.25$ V, and $K_S = (2.06)(25 \times 10^{-6}\ \text{A/V}^2)$

Unknowns: t_f, t_r, τ_{PHL}, τ_{PHL}, and τ_p

Approach: Find t_r and τ_{PLH} using Eqs. (6.52) and (6.53); calculate R_{onS} and use it to evaluate Eq. (6.61) and Eq. (6.66); $\tau_p = (\tau_{PHL} + \tau_{PHL})/2$

Assumptions: R_{onS} is calculated in the triode region.

Analysis: For the resistive load inverter, the rise time and low-to-high propagation delay are

$$t_r = 2.2RC = 2.2(95\ \text{k}\Omega)(0.1\ \text{pF}) = 20.9\ \text{ns}$$

$$\tau_{PLH} = 0.69RC = 0.69(95\ \text{k}\Omega)(0.1\ \text{pF}) = 6.56\ \text{ns}$$

To find t_f and τ_{PHL}, we first calculate the value of R_{onS}:

$$R_{\text{onS}} = \frac{1}{K_S(V_H - V_{TNS})} = \frac{1}{(2.06)\left(25\frac{\mu\text{A}}{\text{V}^2}\right)(5-1)\ \text{V}} = 4.85\ \text{k}\Omega$$

Substituting the data values into Eqs. (6.61) and (6.66):

$$\tau_{PHL} = R_{\text{onS}}C\left\{\ln\left[4\left(\frac{V_H - V_{TNS}}{V_H + V_L}\right) - 1\right] + \frac{2V_{TNS}}{V_H - V_{TNS}}\right\}$$

$$\ln\left[4\left(\frac{5-1}{5+0.25}\right) - 1\right] + \frac{2}{5-1} = 1.22$$

$$\tau_{PHL} = 1.22R_{\text{onS}}C = 1.22(4.85\ \text{k}\Omega)(0.1\ \text{pF}) = 0.590\ \text{ns}$$

$$t_f = t_4 - t_1 = R_{\text{onS}}C\left[\ln\left(\frac{V_H - 2V_{TNS} + 0.9\,\Delta V}{V_H - 0.9\,\Delta V}\right) + 2\left(\frac{V_{TNS} - 0.1\,\Delta V}{V_H - V_{TNS}}\right)\right]$$

$$\ln\left[\frac{5 - 2 + 0.9(4.75)}{5 - 0.9(4.75)}\right] + 2\left(\frac{1 - 0.1(4.75)}{5-1}\right) = 2.57$$

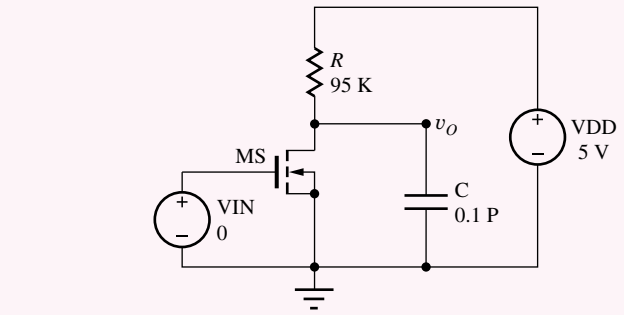
$$t_f = 2.57R_{\text{onS}}C = 2.57(4.85\ \text{k}\Omega)(0.1\ \text{pF}) = 1.25\ \text{ns}$$

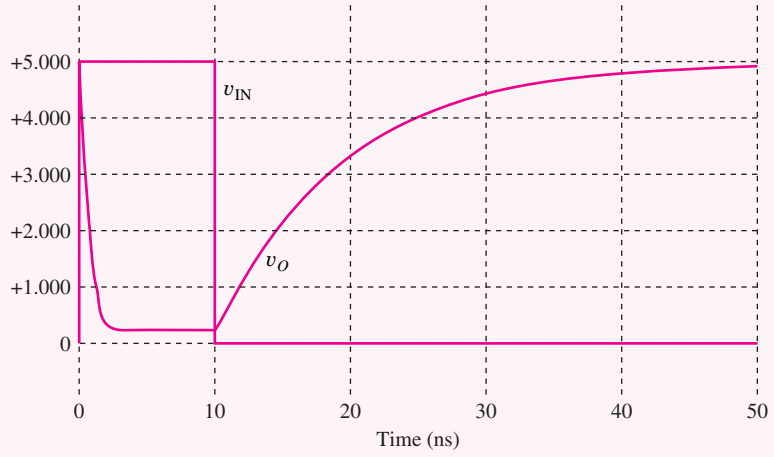
$$\tau_p = \frac{\tau_{PHL} + \tau_{PLH}}{2} = \frac{6.56 + 0.59}{2}\ \text{ns} = 3.58\ \text{ns}$$

Check of Results: A double check of the arithmetic indicates our calculations are correct. We see the expected asymmetry in the rise and fall times as well as in the two propagation delay values. For the on-resistance calculation, $V_{GS} - V_{TN} = 5 - 1 = 4$ V and $V_{DS} = 0.25$ V. ✔

Discussion: Remember that the asymmetry in the rise and fall times and in τ_{PHL} and τ_{PHL} will occur in all single channel technology because the switching device must have a much smaller on-resistance than that of the load in order to produce the desired value of V_L. We see that τ_{PLH} is approximately 11 times τ_{PHL} and that t_r is more than 10 times t_f!

Computer-Aided Analysis: Let us check our hand calculations using the SPICE transient simulation capability. In the circuit schematic, VIN is a pulse source with an initial value of 0, peak value of 5 V, zero delay time, 0.1-ns rise time, 0.1-ns fall time, 9.9-ns pulse width, and a 100-ns period. Note the pulse width is chosen so that the rise time plus the pulse width add up to a convenient value of 10 ns. The rise and fall times for VIN are chosen to be much smaller than those expected for the inverter. The transient simulation parameters are a start time of zero, stop time of 50 ns and a time step of 0.025 ns.





The SPICE results yield values that are very similar to our hand calculations: $t_f = 1.3$ ns, $\tau_{PHL} = 0.64$ ns, $t_r = 21$ ns, and $\tau_{PLH} = 6.3$ ns. (Note: In order to extract these values from the simulation one must expand the scale for the falling portion of the waveform.)

EXERCISE: Recalculate the values of t_f, t_r, τ_{PHL}, τ_{PLH}, and τ_P if C is increased to 0.25 pF.

ANSWERS: 52.3 ns; 16.4 ns; 1.48 ns; 3.13 ns; 8.95 ns

6.14.3 NMOS Inverter with a Depletion-Mode Load

The mathematical complexity of the analysis increases for inverters that use transistors as load elements. For hand calculations, we obtain useful analytical results by neglecting the body effect. If more accurate estimates are needed, they can be obtained using circuit simulation with SPICE. In this section, we will derive estimates of the fall time, rise time, and propagation delay for the depletion-load inverter, which provides the highest performance of the various NMOS inverters.

As mentioned earlier, static NMOS logic gates are "ratioed" designs, in which the current drive capability of the switching transistor must be much greater than that of the load transistor in order to achieve a small value of V_L. Thus, we are always able to assume that the drain current of the switching transistor is much greater than that of the load device ($i_{DS} \gg i_{DL}$) during the high-to-low switching transient, except for v_O very near V_L. Therefore, we can assume that all the drain current of the switching transistor is available to discharge the load capacitance, as in Fig. 6.44.

Fall Time and High-to-Low Propagation Delay Estimates

If we think about the depletion-mode load inverter circuit for a moment, we can save ourselves a lot of work. Since $V_H = V_{DD}$ for the depletion load inverter, the conditions during the high-to-low switching transient are identical to those for the inverter with resistor load. Hence the fall time and propagation delay time on the negative transistion are equivalent to those already presented in Eqs. (6.66) and (6.61):

$$t_f = R_{\text{onS}} C \left[\ln \left(\frac{V_H - 2V_{TNS} + 0.9\,\Delta V}{V_H - 0.9\,\Delta V} \right) + 2 \left(\frac{V_{TNS} - 0.1\Delta V}{V_H - V_{TNS}} \right) \right] \tag{6.67}$$

$$\tau_{PHL} = R_{\text{onS}} C \left\{ \ln \left[4 \left(\frac{V_H - V_{TNS}}{V_H + V_L} \right) - 1 \right] + \frac{2V_{TNS}}{V_H - V_{TNS}} \right\} \tag{6.68}$$

$$R_{\text{onS}} = \frac{1}{K_S(V_H - V_{TNS})}$$

Rise Time and Low-to-High Propagation Delay Estimates

Figure 6.47 shows the inverter with a depletion-mode load. At $t = 0$, the input signal turns off M_S. The current from the source of the load device charges the capacitor from an initial value of V_L to the final value of $V_{DD} = 5$ V. Figure 6.48 shows important times for the low-to-high switching transition for the depletion-mode load case. The times t_1 and t_4 correspond to the 10 percent and 90 percent points on the positive transition and determine the rise time. Time t_3 is the 50 percent point, and $\tau_{PLH} = t_3$, assuming that the input signal is a step function. Time t_2 is the point at which the depletion-mode device comes out of saturation when its drain-source voltage reaches $V_{DS} = -V_{TNL}$ because $V_{GS} = 0$. In this figure, $t_2 < t_3$, but it is possible for $t_3 > t_2$ for some values of V_{TNL}.

Calculation of τ_{PLH}

We begin calculating τ_{PLH} by writing the propagation delay $\tau_{PLH} = t_3$ as

$$\tau_{PLH} = t_2 + (t_3 - t_2) \tag{6.69}$$

because t_2 is the time at which the load device changes regions of operation. The depletion-mode load device operates in saturation for $0 \le t \le t_2$, and is in the triode region for $t > t_2$. The depletion-mode load starts in saturation, and, because $v_{GS} = 0$,

$$i_{DL} = \frac{K_L}{2}(V_{TNL})^2 \tag{6.70}$$

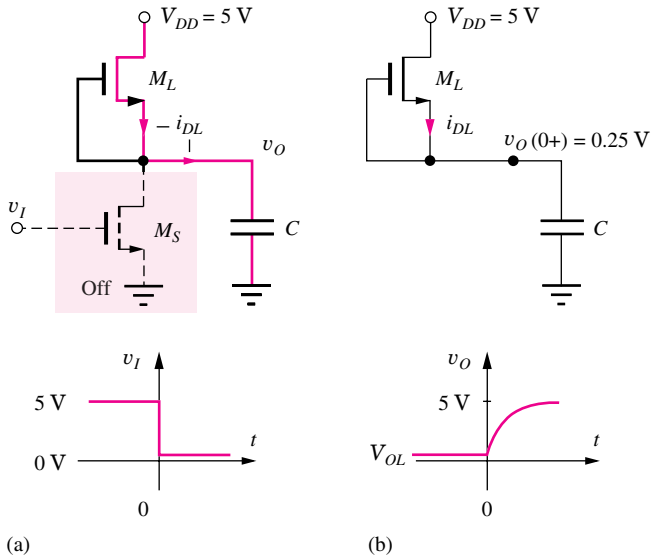


Figure 6.47 Low-to-high switching transient for an inverter with a depletion-mode load device.

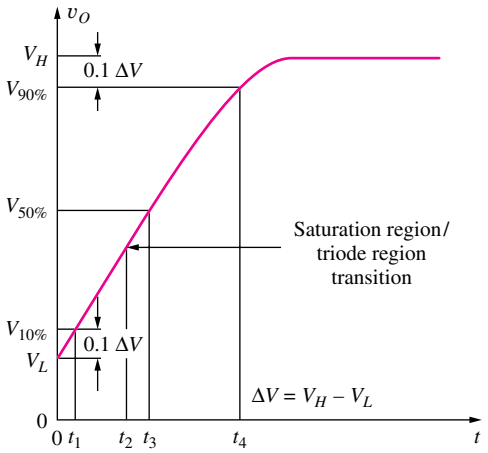


Figure 6.48 Important times in the low-to-high switching transient of an inverter with a depletion-mode load device.

as long as

$$v_{DS} > v_{GS} - V_{TNL} \qquad \text{or} \qquad v_{DS} > -V_{TNL} \text{ because } v_{GS} = 0$$

Because $v_{DS} = V_{DD} - v_O$, we find that the load device will be in saturation for

$$v_O < V_{DD} + V_{TNL}$$

(Remember that $V_{TNL} < 0$ for the depletion-mode device.) Time t_2 is the time required for the transistor to reach the edge of saturation:

$$t_2 = \frac{C}{i_{DL}}[v(t_2) - v(0)] \qquad \text{or} \qquad t_2 = \frac{2C}{K_L(V_{TNL})^2}[V_{DD} + V_{TNL} - V_L] \tag{6.71}$$

During the time interval $t_2 - t_3$, the load device is operating in the triode region, with $v_{GS} = 0$ and $v_{DS} = V_{DD} - v_C$:

$$i_{DL} = K_L\left(0 - V_{TNL} - \frac{V_{DD} - v_C}{2}\right)(V_{DD} - v_C) \tag{6.72}$$

Once again, $i_{DL} = C\dfrac{dv_C}{dt}$, and we have

$$\int_{V_2}^{V_3} \frac{dv_C}{(-2V_{TNL} - (V_{DD} - v_C))(V_{DD} - v_C)} = \int_{t_2}^{t_3} \frac{K_L}{2C}\,dt \tag{6.73}$$

in which $V_2 = V_{DD} + V_{TNL}$ and $V_3 = (V_H + V_L)/2$. Using the result in Eq. (6.59),

$$t_3 - t_2 = R_{\text{onL}}C \ln\left[4\left(\frac{-V_{TNL}}{V_H - V_L}\right) - 1\right] \tag{6.74}$$

where the on-resistance of the depletion-mode device is given by

$$R_{\text{onL}} = \frac{1}{K_L(-V_{TNL})}$$

Finally

$$\tau_{PLH} = (t_3 - t_2) + t_2 = R_{\text{onL}}C\left\{\ln\left[4\left(\frac{-V_{TNL}}{V_H - V_L}\right) - 1\right] + 2\frac{V_H + V_{TNL} - V_L}{(-V_{TNL})}\right\} \tag{6.75}$$

Rise Time Calculation

The rise time is written as

$$t_r = t_4 - t_1 = (t_4 - t_2) - (t_2 - t_1)$$

because the transistor is in saturation during the time between t_1 and t_2, and it is in the triode region from t_2 to t_4. If we define $V_2 = V_C(t_2)$, then $V_2 = V_{DD} + V_{TNL}$. At t_4, the output voltage is at the 90 percent point and

$$V_{90\%} = V_H - 0.1\,\Delta V$$

Once again using Eq. (6.59) and more algebra,

$$t_4 - t_2 = R_{\text{onL}}C\ln\left[\left(-\frac{20V_{TNL}}{\Delta V}\right) - 1\right] \tag{6.76}$$

and

$$t_2 - t_1 = \frac{2C}{K_L(V_{TNL})^2}[V_H + V_{TNL} - (V_L + 0.1\,\Delta V)] \tag{6.77}$$

Combining Eqs. (6.76) and (6.77) gives the rise time

$$t_r = R_{\text{onL}}C\left\{\ln\left[\left(-\frac{20V_{TNL}}{\Delta V}\right) - 1\right] + 2\frac{V_H + V_{TNL} - V_L - 0.1\,\Delta V}{(-V_{TNL})}\right\} \tag{6.78}$$

Let us look at the time responses a bit further by evaluating the various expressions with $V_H = V_{DD} = 5$ V, $V_L = 0.25$ V, $V_{TNS} = 1$ V, and $V_{TNL} = -3$ V for which we find

$$t_r = 3.3R_{\text{onL}}C \qquad t_f = 2.57R_{\text{onS}}C \qquad \tau_{PLH} = 1.59R_{\text{onL}}C \qquad \tau_{PHL} = 1.22R_{\text{onS}}C$$

$$R_{\text{onL}} = \frac{1}{3K_L} \qquad R_{\text{onS}} = \frac{1}{4K_S}$$

First, we observe that the expressions are all proportional to load capacitance C and the on-resistance of either the load transistor or the switching transistor. The specific constants multiplying the RC terms differ somewhat from those describing the resistor load inverter, illustrating their dependence on the details of the technology. In these equations, we see that the depletion load inverter has more symmetric values for the two propagation delays.

EXAMPLE 6.12 **DYNAMIC PERFORMANCE OF THE INVERTER WITH A DEPLETION-MODE LOAD**

Evaluate the expressions describing the temporal response of the depletion-load inverter.

PROBLEM Find τ_{PLH}, τ_{PHL}, τ_P, t_r, and t_f for the inverter with a depletion-mode load from Fig. 6.32(d) with a load capacitance $C = 0.1$ pF. Ignore body effect.

SOLUTION **Known Information and Given Data:** Depletion-load inverter in Fig. 6.32(d) with $C = 0.1$ pF, $V_{TNS} = 1$ V, $V_{DD} = 5$ V, $V_{TNL} = -3$ V, $V_L = 0.25$ V, $K_S = (2.06)(25 \times 10^{-6}$ A/V$^2)$, and $K_L = (25 \times 10^{-6}$ A/V$^2)/2.15$.

Unknowns: t_f, t_r, τ_{PHL}, τ_{PHL}, and τ_P

Approach: Use known data to evaluate Eqs. (6.67), (6.68), (6.75), and (6.78) and $\tau_P = (\tau_{PHL} + \tau_{PHL})/2$

Assumptions: Body effect in the load device is neglected in the equations. $V_H = V_{DD}$.

Analysis: The known data values are substituted into Eqs. (6.67), (6.68), (6.75), and (6.78): The high-to-low propagation delay is found using the on-resistance of the switch:

$$R_{\text{onS}} = \frac{1}{K_S(V_H - V_{TNS})} = \frac{1}{(2.06)\left(25\dfrac{\mu\text{A}}{\text{V}^2}\right)(5-1)} = 4.85\ \text{k}\Omega$$

$$\tau_{PHL} = R_{\text{onS}}C\left\{\ln\left[4\left(\frac{V_H - V_{TNS}}{V_H + V_L}\right) - 1\right] + \frac{2V_{TNS}}{V_H - V_{TNS}}\right\}$$

$$\tau_{PHL} = R_{\text{onS}}C\left\{\ln\left[4\left(\frac{5-1}{5+0.25}\right) - 1\right] + \frac{2(1)}{5-1}\right\} = 1.22R_{\text{onS}}C$$

$$\tau_{PHL} = 1.22(4.85\ \text{k}\Omega)(0.1\ \text{pF}) = 0.590\ \text{ns}$$

For this inverter, the logic swing is $\Delta V = V_H - V_L = 4.75$ V, and the fall time is

$$t_f = R_{\text{onS}}C\left\{\ln\left[\frac{V_H - 2V_{TNS} + 0.9\,\Delta V}{V_H - 0.9\,\Delta V}\right] + 2\left(\frac{V_{TNS} - 0.1\,\Delta V}{V_H - V_{TNS}}\right)\right\}$$

$$t_f = R_{\text{onS}}C\left\{\ln\left[\frac{5 - 2 + 0.9(4.75)}{5 - 0.9(4.75)}\right] + 2\left(\frac{1 - 0.1(4.75)}{5-1}\right)\right\} = 2.57R_{\text{onS}}C$$

$$t_f = 2.57(4.85\ \text{k}\Omega)(0.1\ \text{pF}) = 1.25\ \text{ns}$$

The low-to-high propagation delay is

$$\tau_{PLH} = R_{\text{onL}}C\left\{\ln\left[4\left(\frac{-V_{TNL}}{V_H - V_L}\right) - 1\right] + 2\frac{V_H + V_{TNL} - V_L}{(-V_{TNL})}\right\} \qquad R_{\text{onL}} = \frac{1}{K_L(-V_{TNL})}$$

$$\ln\left[4\left(\frac{3}{5-0.25}\right) - 1\right] + 2\frac{5-3-0.25}{3} = 1.59 \qquad R_{\text{onL}} = \frac{1}{\left(\dfrac{25}{2.15}\ \mu\text{A/V}^2\right)(3)} = 28.7\ \text{k}\Omega$$

$$\tau_{PLH} = 1.59R_{\text{onL}}C = 1.59(28.7\ \text{k}\Omega)(0.1\ \text{pF}) = 4.56\ \text{ns}$$

and the rise time is calculated as

$$t_r = R_{\text{onL}}C\left\{\ln\left[\left(-\frac{20V_{TNL}}{\Delta V}\right) - 1\right] + 2\frac{V_H + V_{TNL} - V_L - 0.1\,\Delta V}{(-V_{TNL})}\right\}$$

$$t_r = R_{\text{onL}}C\left\{\ln\left[\left(-\frac{20(-3)}{4.75}\right) - 1\right] + 2\frac{5-3-0.25-0.475}{3}\right\} = 3.30R_{\text{onL}}C$$

$$t_r = 3.30(28.7\ \text{k}\Omega)(0.1\ \text{pF}) = 9.47\ \text{ns}$$

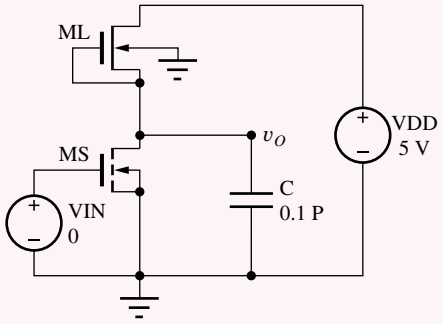
Finally, the average propagation delay is given by

$$\tau_p = \frac{\tau_{PHL} + \tau_{PLH}}{2} = \frac{0.590 + 4.56}{2} \text{ ns} = 2.58 \text{ ns}$$

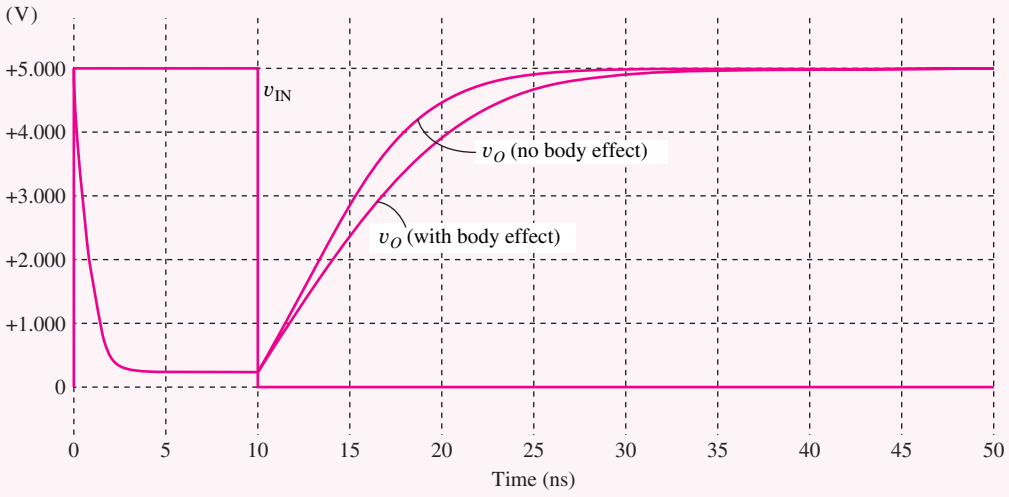
Check of Results: A double check of the arithmetic indicates our calculations are correct. We observe the expected asymmetry in the rise and fall times as well as in the two propagation delay values

Discussion: We see that τ_{PLH} is approximately 5 times t_{PHL} and also that the rise time is much longer than the fall time. These results are consistent with our assumption that we can neglect the load device current with respect to the switching device current during the high-to-low transition.

Computer-Aided Analysis: Let's compare our hand calculations using the SPICE transient simulation capability. In the circuit schematic, VIN is a pulse source with an initial value of 0, a peak value of 5 V, zero delay time, 0.1-ns rise time, 0.1-ns fall time, 9.9-ns pulse width, and a 100-ns period. Note the pulse width is chosen so that the rise time plus the pulse width add up to a convenient value of 10 ns. The rise and fall times for VIN are chosen to be much smaller than those expected for the inverter. The transient simulation parameters are a start time of zero, a stop time of 50 ns, and a time step of 0.025 ns.



The SPICE results without body effect yield values that are quite similar to our hand calculations: $t_f = 1.4$ ns, $\tau_{PHL} = 0.60$ ns, $t_r = 9.5$ ns, and $\tau_{PLH} = 4.5$ ns. In the second output curve, we see that body effect degrades both the propagation delay and rise time. The values increase to $t_r = 13.7$ ns and $\tau_{PLH} = 5.6$ ns.



EXERCISE: Suppose we double the size of both transistors in the inverter: $(W/L)_S = 4.12/1$ and $(W/L)_L = 1/1.08$. What are the new values of t_f, t_r, τ_{PLH}, τ_{PHL}, and τ_P. What is the new power dissipation of the logic gate for $v_O = V_L$?

ANSWERS: 0.63 ns; 4.7 ns; 2.3 ns; 0.30 ns; 1.3 ns; 0.50 mW

6.14.4 NMOS INVERTER WITH A SATURATED LOAD

In order to see a good comparison of the various NMOS inverters, we need the time responses for the saturated load inverter. We will just state the results here. The analyses are similar to those for the resistor load and depletion load inverter, and the detailed calculations can be found on the **MCD website.** A primary difference to keep in mind is that the value of V_H is no longer equal to power supply voltage V_{DD}.

$$\tau_{PHL} = R_{\text{onS}}C\left\{\ln\left[4\left(\frac{V_H - V_{TNS}}{V_H + V_L}\right) - 1\right] + \frac{2V_{TNS}}{V_H - V_{TNS}}\right\}$$

$$t_f = R_{\text{onS}}C\left[\ln\left(\frac{V_H - 2V_{TNS} + 0.9\,\Delta V}{V_H - 0.9\,\Delta V}\right) + 2\left(\frac{V_{TNS} - 0.1\,\Delta V}{V_H - V_{TNS}}\right)\right] \qquad (6.79)$$

$$\tau_{PLH} = 2R_{\text{onL}}C \qquad t_r = \frac{160}{9}R_{\text{onL}}C$$

$$R_{\text{onL}} = \frac{1}{K_L(V_H - V_L)} \qquad R_{\text{onS}} = \frac{1}{K_S(V_H - V_{TNS})}$$

Let us evaluate these expressions with numbers from our 5-V design, $V_H = 3.39$ V, $V_L = 0.25$ V, and $V_{TNS} = 1$ V, for which we find

$$t_r = 17.8R_{\text{onL}}C \qquad t_f = 2.61R_{\text{onS}}C \qquad \tau_{PLH} = 2.00R_{\text{onL}}C \qquad \tau_{PHL} = 1.36R_{\text{onS}}C$$

$$R_{\text{onL}} = \frac{1}{3.14K_L} \qquad R_{\text{onS}} = \frac{1}{2.39K_S}$$

Once again, we observe that the expressions are all proportional to load capacitance C and the on-resistance of either the load transistor or the switching transistor. The specific constants multiplying the RC terms are again dependent on the details of the technology, but one large difference does stand out. The rise time is significantly larger than the other forms of inverters, and this occurs because the current of the saturated load device decreases quadratically as the output voltage rises toward V_H. In effect, the on-resistance of the load transistor increases dramatically as v_O gets closer to V_H. Note, however, that the propagation delay time (the time to the 50 percent point) is only lengthened slightly compared to the depletion-load inverter.

EXAMPLE 6.13 DYNAMIC PERFORMANCE OF A SATURATED LOAD INVERTER

Here we calculate numeric values for the dynamic performance of an NMOS inverter with a saturated load device.

PROBLEM Find τ_{PLH}, τ_{PHL}, τ_P, t_r, and t_f for the inverter with a saturated load from Fig. 6.32 with a load capacitance $C = 0.1$ pF.

SOLUTION **Known Information and Given Data:** Saturated load inverter in Fig. 6.32(b) with $C = 0.1$ pF, $V_{DD} = 5$ V, $V_H = 3.39$ V, $V_L = 0.25$ V, and $K_S = (3.53)(25 \times 10^{-6}\ \text{A/V}^2)$, $K_L = (25\ \mu\text{A/V}^2)/3.39$

Unknowns: t_f, t_r, τ_{PHL}, τ_{PHL}, and τ_P

Approach: Use known data to calculate R_{onS} and R_{onL} and to evaluate Eqs. (6.79). Then $\tau_P = (\tau_{PHL} + \tau_{PHL})/2$

Assumptions: Body effect in the load device was neglected in the equations. However, we will use the up-level calculation including body-effect to get a more realistic estimate of t_r and τ_{PLH}.

Analysis: We now substitute the known data values into Eqs. (6.79). The high-to-low propagation delay is found using the on-resistance of the switch:

$$R_{\text{onS}} = \frac{1}{K_S(V_H - V_{TNS})} = \frac{1}{(3.53)(25\ \mu\text{A/V}^2)(3.39 - 1)\ \text{V}} = 4.74\ \text{k}\Omega$$

$$\tau_{PHL} = R_{\text{onS}}C\left\{\ln\left[4\left(\frac{V_H - V_{TNS}}{V_H + V_L}\right) - 1\right] + \frac{2V_{TNS}}{V_H - V_{TNS}}\right\}$$

$$\tau_{PHL} = R_{\text{onS}}C\left\{\ln\left[4\left(\frac{3.39 - 1}{3.39 + 0.25}\right) - 1\right] + \frac{2(1)}{3.39 - 1}\right\} = 1.36R_{\text{onS}}C$$

$$\tau_{PHL} = 1.36R_{\text{onS}}C = 1.36(4.74\ \text{k}\Omega)(0.1\ \text{pF}) = 0.645\ \text{ns}$$

For this inverter, the logic swing $\Delta V = 3.39 - 0.25 = 3.14$ V, and the fall time is

$$t_f = R_{\text{onS}}C\left\{\ln\left(\frac{V_H - 2V_{TNS} + 0.9\,\Delta V}{V_H - 0.9\,\Delta V}\right) + 2\left(\frac{V_{TNS} - 0.1\,\Delta V}{V_H - V_{TNS}}\right)\right\}$$

$$t_f = R_{\text{onS}}C\left\{\ln\left(\frac{3.39 - 2(1) + 0.9(3.14)}{3.39 - 0.9(3.14)}\right) + 2\left(\frac{1 - 0.1(3.14)}{3.39 - 1}\right)\right\}$$

$$t_f = 2.61R_{\text{onS}}C = 2.61(4.74\ \text{k}\Omega)(0.1\ \text{pF}) = 1.24\ \text{ns}$$

The low-to-high propagation delay and the rise time are found to be

$$\tau_{PLH} = 2R_{\text{onL}}C \qquad R_{\text{onL}} = \frac{1}{K_L(V_H - V_L)} = \frac{1}{\left(\frac{25\ \mu\text{A/V}^2}{3.39}\right)(3.39 - 0.25)\ \text{V}} = 43.2\ \text{k}\Omega$$

$$\tau_{PLH} = 2R_{\text{onL}}C = 2(43.2\ \text{k}\Omega)(0.1\ \text{pF}) = 8.64\ \text{ns}$$

$$t_r = \frac{160}{9}R_{\text{onL}}C = 17.8(43.2\ \text{k}\Omega)(0.1\ \text{pF}) = 76.9\ \text{ns}$$

Finally, the average propagation delay is given by

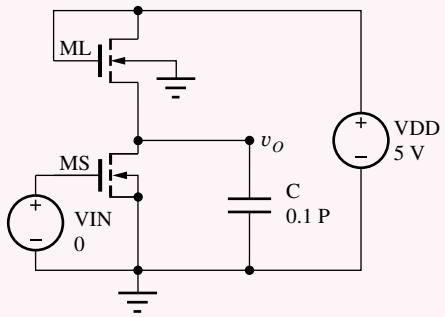
$$\tau_p = \frac{\tau_{PHL} + \tau_{PLH}}{2} = \frac{0.645 + 8.64}{2}\ \text{ns} = 4.64\ \text{ns}$$

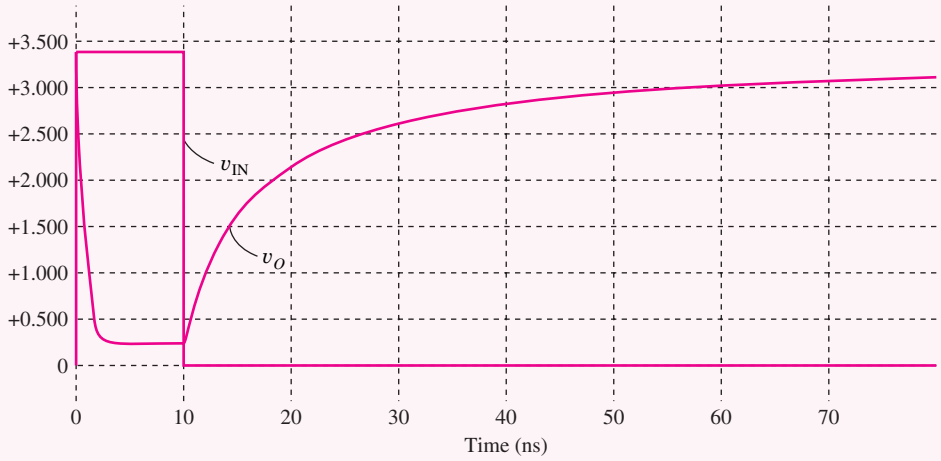
Check of Results: A double check of the arithmetic indicates our calculations are correct. We see the expected asymmetry in the rise and fall times as well as in the two propagation delay values.

Discussion: We see that τ_{PLH} is an order of magnitude greater than t_{PHL} and also that the rise time is much longer than the fall time. These results are consistent with our assumption that we can neglect the load device current with respect to the switching device current during the

high-to-low transition. As mentioned earlier, the rise time is much greater than τ_{PLH} because the pull-up transient takes a long time to approach final value as the saturated load device approaches cutoff.

Computer-Aided Analysis: Let's compare our hand calculations using the SPICE transient simulation capability. In the circuit schematic, VIN is a pulse source with an initial value of 0, a peak value of 3.39 V, zero delay time, 0.1-ns rise time, 0.1-ns fall time, 9.9-ns pulse width, and a 100-ns period. Note the pulse width is chosen so that the rise time plus the pulse width add up to a convenient value of 10 ns. The rise and fall times for VIN are chosen to be much smaller than those expected for the inverter. The transient simulation parameters are a start time of zero, stop time of 80 ns, and a time step of 0.025 ns.





The SPICE results yield values that are similar to our hand calculations: $t_f = 1.5$ ns, $\tau_{PHL} = 0.65$ ns, $t_r = 62$ ns, and $\tau_{PLH} = 6.5$ ns. The largest discrepancies are on the rising transition where our formulas are over estimating the effective value of R_{onL}. On the rising transition, note that the waveform reaches the 50 percent point relatively quickly, but a long time is required to go from the 50 percent point to the 90 percent point. As mentioned previously, this long tail represents another one of the problems with saturated load logic.

EXERCISE: Recalculate the values of t_f, t_r, τ_{PHL}, τ_{PLH}, and τ_P if C is increased to 0.25 pF.

ANSWERS: 3.10 ns; 192 ns; 1.61 ns; 21.6 ns; 11.6 ns

6.15 A FINAL COMPARISON OF LOAD DEVICES

Figure 6.49 is a comparison of the i-v characteristics of the various load devices that we have studied, with and without the influence of body effect on the transistor characteristics. The device sizes have been chosen so that the output current in each load is 50 μA when v_O is at the output low level of 0.25 V. As a reference for comparison, curve (e) is the straight line corresponding to the constant 95-kΩ load resistor.

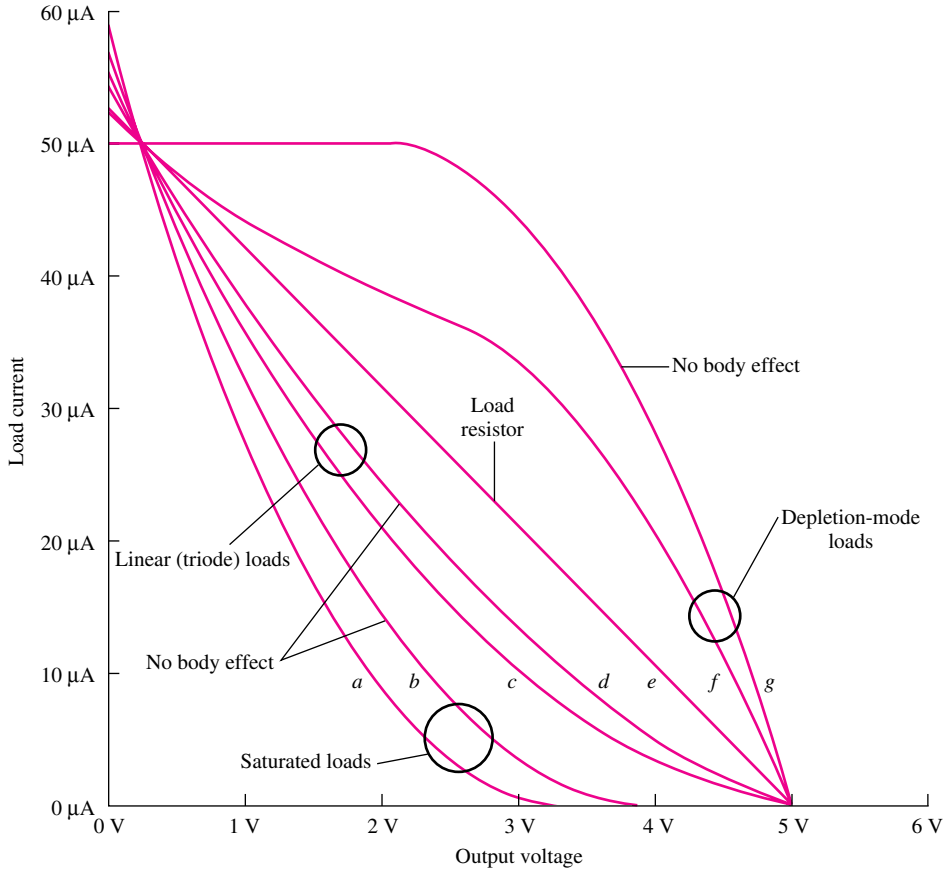


Figure 6.49 A comparison of NMOS load device characteristics with current normalized to 50 μA for $v_o = V_{OL} = 0.25$ V: (a) saturated load device including body effect, (b) saturated load device with no body effect, (c) linear (triode) load device including body effect, (d) linear (triode) load device with no body effect, (e) 95-kΩ resistor load, (f) depletion-mode load device including body effect, (g) depletion-mode load device without body effect.

For all the MOS load device cases, body effect degrades the performance of the load device. Both saturated load characteristics, (*a* and *b* in Fig. 6.49) deliver substantially less current than the resistor throughout the full output voltage transition. Thus, we expect gates with saturated loads to have the poorest values of τ_{PLH}. We also can observe that the load current of the saturated load devices goes to zero before the output reaches 5 V. The linear loads *c* and *d* are an improvement over the saturated load devices but still provide less current than the resistive load. The depletion-mode load devices *f* and *g* provide the largest current throughout the transition, and thus they should exhibit the smallest value of τ_{PLH}. The ideal depletion-mode load *g* functions as a current source for $v_O < 2.1$ V. Note, however, that body effect substantially degrades the current source characteristics of the depletion-mode device.

TABLE 6.13
Summary of Dynamic Responses of NMOS Inverters

***t_f* and *τ_{PHL}*:** The expressions for fall time t_f and high-to-low propagation delay τ_{PHL} are the identical for all the inverters (Remember, however, that the values of V_H and V_L are circuit dependent):

$$t_f = R_{\text{onS}}C\left[\ln\left(\frac{V_H - 2V_{TNS} + 0.9\,\Delta V}{V_H - 0.9\,\Delta V}\right) + 2\left(\frac{V_{TNS} - 0.1\,\Delta V}{V_H - V_{TNS}}\right)\right]$$

$$\tau_{PHL} = R_{\text{onS}}C\left\{\ln\left[4\left(\frac{V_H - V_{TNS}}{V_H + V_L}\right) - 1\right] + \frac{2V_{TNS}}{V_H - V_{TNS}}\right\}$$

$$R_{\text{onS}} = \frac{1}{K_S(V_H - V_{TNS})}$$

***t_r* and *τ_{PLH}*:** The expressions for rise time t_r and low-to-high propagation delay τ_{PLH} depend on the load device. ($\Delta V = V_H - V_L$.)

Resistor load:

$$t_r = 2.2RC \qquad \text{and} \qquad \tau_{PLH} = 0.69RC$$

Saturated load:

$$t_r = \frac{160}{9}R_{\text{onL}}C \qquad \text{and} \qquad \tau_{PLH} = 2R_{\text{onL}}C$$

$$R_{\text{onL}} = \frac{1}{K_L(V_H - V_L)} = \frac{1}{K_L(\Delta V)}$$

Depletion-mode load:

$$t_r = R_{\text{onL}}C\left\{\ln\left[20\frac{(-V_{TNL})}{\Delta V} - 1\right] + 2\frac{0.9\,\Delta V + V_{TNL}}{(-V_{TNL})}\right\}$$

$$\tau_{PLH} = R_{\text{onL}}C\left\{\ln\left[4\frac{(-V_{TNL})}{\Delta V} - 1\right] + 2\frac{\Delta V + V_{TNL}}{(-V_{TNL})}\right\}$$

$$R_{\text{onL}} = \frac{1}{K_L(-V_{TNL})}$$

In our hand calculations, we neglected body effect. Based on the curves in Fig. 6.49, we can expect that the equations that were derived for t_f and τ_{PHL} may show substantial disagreement with actual measurements. This figure reinforces the need for circuit simulation if detailed analysis of digital logic circuits is required.

Table 6.13 collects together the delay equations derived for the various inverters analyzed in Sec. 6.14. The equations provide reasonable first-order estimates of the time responses of the various forms of NMOS inverters. Although, the equations appear somewhat cumbersome, they can be reduced to much simpler form once the circuit voltage parameters have been selected (i.e., V_{DD}, V_{TN}, V_L, ΔV, etc.). Table 6.14 provides such a reduction for the 5-V designs that were analyzed in Sec. 6.14.

Each of the time responses is determined by an RC product consisting of the load capacitance and on-resistance of the switch or load transistor. The constants in front of the RC terms are determined by the various circuit voltages, although they are not strong functions of the voltages due to logarithmic dependencies.

Note that the time responses are inversely proportional to carrier mobility since the on-resistances contain mobility in K_S and K_L. Thus, we expect NMOS logic to be approximately

TABLE 6.14
Simplified Inverter Temporal Responses*

	RESISTOR LOAD	SATURATED LOAD	DEPLETION-MODE LOAD
τ_{PHL}	$1.2R_{\text{onS}}C$	$1.4R_{\text{onS}}C$	$1.2R_{\text{onS}}C$
t_f	$2.6R_{\text{onS}}C$	$2.6R_{\text{onS}}C$	$2.6R_{\text{onS}}C$
τ_{PLH}	$0.69RC$	$2.0R_{\text{onL}}C$	$1.6R_{\text{onL}}C$
t_r	$2.2RC$	$18R_{\text{onL}}C$	$3.3R_{\text{onL}}C$

$$R_{\text{onS}} = \frac{1}{K_S(V_H - V_{TNS})} \qquad R_{\text{onL}} = \frac{1}{K_L(V_{GSL} - V_{TNL})}$$

where V_{GSL} is the gate-source voltage of the load device at the beginning of the low-high transition.

*Coefficients calculated for $V_{DD} = 5$ V, $V_L = 0.25$ V, $V_{TN} = 1$ V for enhancement-mode devices, $V_{TN} = -3$ V for depletion-mode transistors. Body effect is ignored.

2.5 times faster than PMOS circuits operating at equivalent voltages. This fact was the main reason for the rapid switch to NMOS technology from PMOS as soon as the manufacturing problems were overcome. Note the approximate $2\times$ relationship between t_f and t_{PHL} for all three inverters. A similar relationship applies to t_r and t_{PLH} for the depletion-load inverter. We will make use of this factor of two relationship in our design of CMOS inverters in Chapter 7.

Figures 6.50 and 6.51 present the results of circuit simulations of the response of the three types of inverters including body effect. It can be seen in Fig. 6.50 that the fall times and propagation delay times of the various inverter configurations are all similar, because the current in the switching transistor is the primary factor determining the characteristics of these waveforms. Much greater differences appear in the waveforms in Fig. 6.51 because of the large differences in the currents supplied by the load devices.

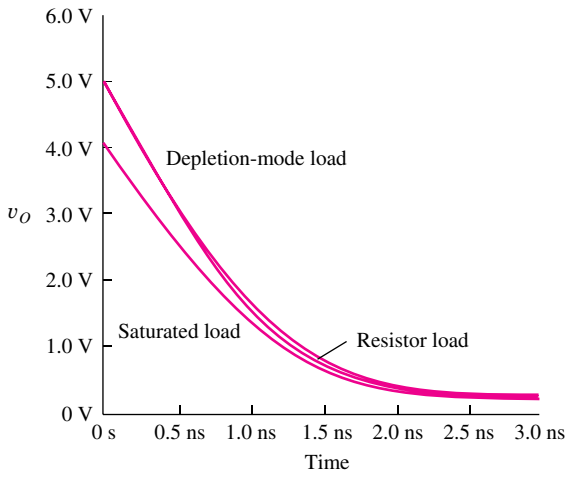


Figure 6.50 SPICE simulation results for fall time and τ_{PHL} for the inverters with resistor load, saturated load, and depletion-mode load for a load capacitance $C = 0.1$ pF.

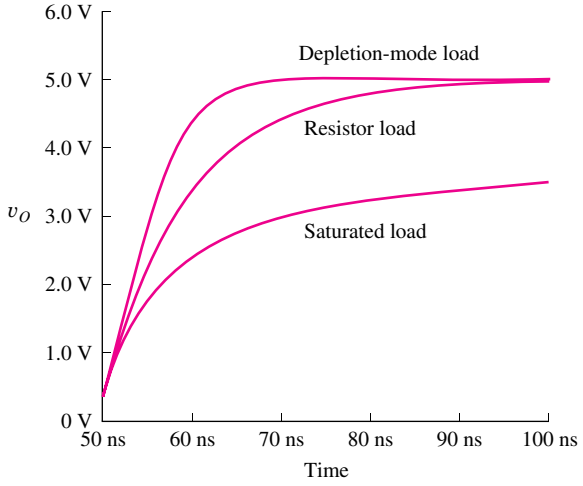


Figure 6.51 SPICE simulation results for rise time and τ_{PLH} for the inverters with resistor load, saturated load, and depletion-mode load for a load capacitance $C = 0.1$ pF.

TABLE 6.15
Analytical Inverter Delay Estimates ($C = 0.1$ pF)

	τ_{PHL}	τ_{PLH}	τ_P	t_f	t_r
Resistor load	0.6 ns	6.6 ns	3.7 ns	1.3 ns	21.0 ns
Saturated load	0.6 ns	8.6 ns	4.6 ns	1.2 ns	77.0 ns
Depletion-mode load	0.6 ns	4.6 ns	2.6 ns	1.2 ns	9.6 ns

TABLE 6.16
SPICE Simulation of Inverter Delays Including Body Effect ($C = 0.1$ pF)

	τ_{PHL}	τ_{PLH}	τ_P	t_f	t_r
Resistor load	0.8 ns	6.6 ns	3.7 ns	1.3 ns	21 ns
Saturated load	0.4 ns	6.5 ns	3.5 ns	1.1 ns	65 ns
Depletion-mode load	0.7 ns	5.5 ns	3.1 ns	1.5 ns	13 ns

Tables 6.15 and 6.16 contain values of inverter delay based on the delay equations and the SPICE simulation results. The results of our hand calculations are surprisingly good. The biggest discrepancy appears in the rise time estimate for the depletion-mode load device, but this should not be a surprise after seeing the results in Fig. 6.49. We see that the depletion-mode load provides the best propagation delay and that the saturated load is similar to a gate with a resistor load, except for the long rise time.

DESIGN EXAMPLE 6.14

PROPAGATION DELAY DESIGN FOR AN INVERTER

The logic gates that drive signals off an integrated-circuit chip are typically loaded by relatively large capacitances. This example determines the size of an inverter that is required to drive a large load capacitor with a small value of propagation delay.

PROBLEM Design a depletion-load inverter to provide an average propagation delay of 2 ns when driving a 10-pF capacitor. Use the reference inverter design in Fig. 6.32 as described by the equations in Tables 6.13 and 6.14. Find the rise and fall times for the logic gate.

Known Information and Given Data: Depletion-mode reference inverter design in Fig. 6.32(d) with $C = 10$ pF, $V_{DD} = 5$ V, $K_n' = 25\ \mu\text{A/V}^2$, $V_{TNS} = 1$ V, $V_{TNL} = -3$ V, $V_H = 5$ V, $V_L = 0.25$ V, $(W/L)_S = 2.06/1$, and $(W/L)_L = 1/2.15$

Unknowns: $(W/L)_S$, $(W/L)_L$, t_f, and t_r

Approach: Use the results in Table 6.14 to find the required values of R_{onL} and R_{onS}. Determine the W/L ratios from the on-resistance values and the reference inverter design.

Assumptions: Remember that body effect in the load device was neglected in the equations derived for the propagation delay of this circuit.

SOLUTION **Method 1:** Using the equations in Table 6.14 for the depletion-mode inverter, we can write an expression for the average propagation delay.

$$\tau_P = \frac{1.2R_{\text{onS}}C + 1.6R_{\text{onL}}C}{2} = \frac{C}{2K_L}\left[\frac{1.2}{\frac{K_S}{K_L}(V_H - V_{TNS})} + \frac{1.6}{(V_{GSL} - V_{TNL})}\right]$$

From the reference inverter we have $K_S/K_L = 2.06(2.15) = 4.43$. Solving for K_L and the W/L ratios of the two transistors yields

$$K_L = \frac{10\text{ pF}}{2(2\text{ ns})}\left[\frac{1.2}{4.43(5-1)} + \frac{1.6}{(0+3)}\right] = 1.503 \times 10^{-3}\frac{\text{A}}{\text{V}^2}$$

$$\left(\frac{W}{L}\right)_L = \frac{K_L}{25\frac{\mu\text{A}}{\text{V}^2}} = \frac{60.1}{1} \qquad \left(\frac{W}{L}\right)_S = 4.43\left(\frac{W}{L}\right)_L = \frac{266}{1}$$

The rise and fall times can also be estimated using the equations in Table 6.14:

$$t_r = \frac{3.3(10\text{ pF})}{60.1\left(25\frac{\mu\text{A}}{\text{V}^2}\right)(3\text{ V})} = 7.32\text{ ns} \quad \text{and} \quad t_f = \frac{2.6(10\text{ pF})}{266\left(25\frac{\mu\text{A}}{\text{V}^2}\right)(5-1)\text{ V}} = 0.977\text{ ns}$$

Method 2: An alternate approach is based on our knowledge of how the delay scales with inverter size, and if we are careful, we can also include the influence of body effect. From the simulation results in Table 6.16 we see that τ_P for the reference depletion-load inverter is 3.1 ns when driving a 0.1-pF capacitor. We desire a 2-ns delay for a 10-pF load capacitor. Thus the transistor sizes must be increased by a scale factor of $\alpha = (3.1\text{ ns}/2\text{ ns})(10\text{ pF}/0.1\text{ pF}) = 155$. The new transistor sizes are $(W/L)_S = 155(2.06/1) = 319/1$ and $(W/L)_L = 155(1/2.15) = 72.1/1$. We see that the device sizes must be increased to account for the delay degradation that results from body effect in the load transistor.

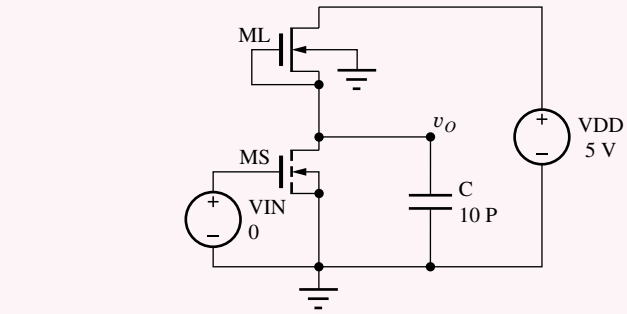
The rise and fall times can be found by scaling the results in Table 6.16. (Remember that we are increasing the speed of the gate relative to the reference design.)

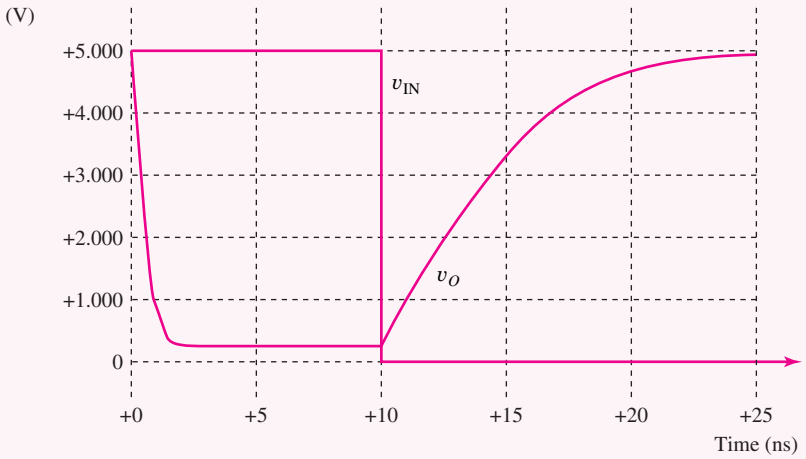
$$t_r = 13\text{ ns}\left(\frac{2\text{ ns}}{3.1\text{ ns}}\right) = 8.4\text{ ns} \quad \text{and} \quad t_f = 1.5\text{ ns}\left(\frac{2\text{ ns}}{3.1\text{ ns}}\right) = 0.97\text{ ns}$$

Check of Results: We have found the unknowns, and the values appear reasonable. The best check will be to simulate the transient response of the new inverter design using SPICE.

Discussion: Large transistor sizes are required to achieve the low propagation delay with a large capacitive load. The input capacitance to this inverter will also be large and require another large driver stage. The optimum form of these "cascade" buffers will be described in Chapter 7.

Computer-Aided Analysis: Now we confirm the behavior of our design using SPICE transient simulation. In the circuit schematic, VIN is a pulse source with initial value of 0, peak value of 5 V, zero delay time, 0.05-ns rise time, 0.05-ns fall time, 9.9-ns pulse width, and a 25-ns period. The pulse width is chosen so that the rise time plus the pulse width add up to a convenient value of 10 ns. The rise and fall times for VIN are chosen to be much smaller than the expected values of the inverter rise and fall times. The transient simulation parameters are a start time of zero, a stop time of 25 ns, and a time step of 0.025 ns.





From the graph of the transient response, we find $\tau_{PHL} = 0.42$ ns and $\tau_{PLH} = 3.6$ ns, yielding $\tau_P = 2.0$ ns. The rise and fall times are 8.8 ns and 1.0 ns, respectively. The values all agree well with the design goals and estimates. Note that had we used the formula values, our gate would have been slower by approximately 16 percent.

EXERCISE: What is the static power dissipation in the inverter in Ex. 6.14? What is the dynamic power dissipation if the inverter is switching on and off every 2 ns?

ANSWERS: 38.8 mW; 125 mW!

EXERCISE: What would be the transistor sizes in Ex. 6.14 if the inverter was required to drive 20 pF with an average propagation delay of 1 ns (a 1-GHz rate)? What is the dynamic power consumption of this inverter?

ANSWERS: 1280/1; 288/1; 0.5 W

6.16 PMOS LOGIC

In the previous sections of this chapter, we have concentrated on understanding NMOS logic circuits. However, as already mentioned several times, PMOS logic historically preceeded NMOS

logic, but was quickly replaced by the higher-performance NMOS logic as soon as NMOS technology could be reliably manufactured. This section presents a brief discussion of PMOS logic circuits.

6.16.1 PMOS Inverters

PMOS logic circuits mirror those presented for NMOS logic as exhibited in Fig. 6.52 which presents the PMOS equivalents of the inverter designs in Fig. 6.32. In these circuits, the power supply has been changed to -5 V and each NMOS transistor has been replaced with a PMOS device.

Each circuit has been designed to have the same power level as the equivalent NMOS circuit: $P = 0.25$ mW. Note that for the circuit in Fig. 6.52(a), $V_L = -5$ V and $V_H = -0.25$ V. In the saturated load circuit in Fig. 6.52(b), $V_L = -4$ V and $V_H = -0.25$ V, assuming the value of $V_{TP} = -1$ V. The W/L ratios have been found by simply scaling the W/L ratios of the NMOS inverters by the mobility ratio $\mu_n/\mu_p = 2.5$, not by going through detailed calculations.

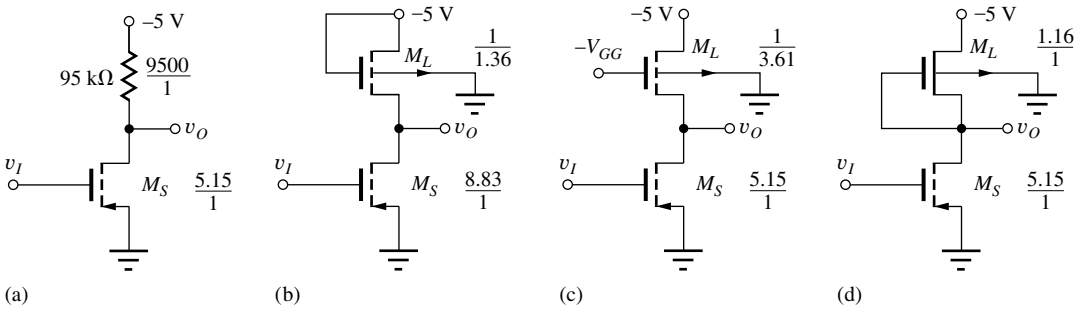


Figure 6.52 PMOS inverters: (a) resistive load, (b) saturated load, (c) linear load, and (d) depletion-mode load.

6.16.2 NOR and NAND Gates

The PMOS NOR and NAND gates in Fig. 6.53 mirror the NMOS circuits in Figs. 6.33 and 6.34. The power supply has been changed to -5 V, and each NMOS transistor has been replaced with a PMOS device. The W/L ratios are scaled by the mobility ratio of 2.5, as described in Sec. 6.15.

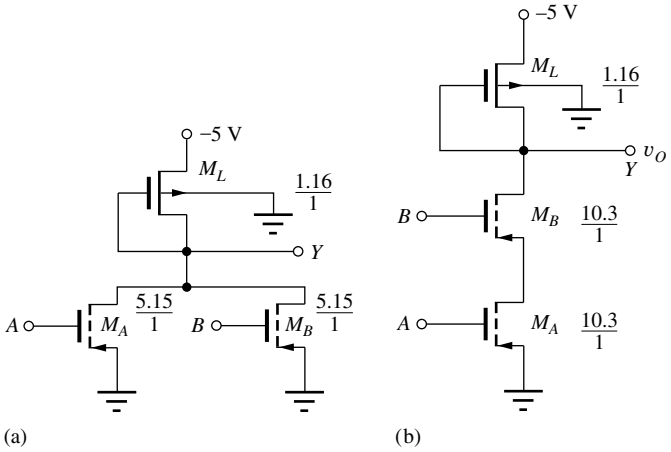


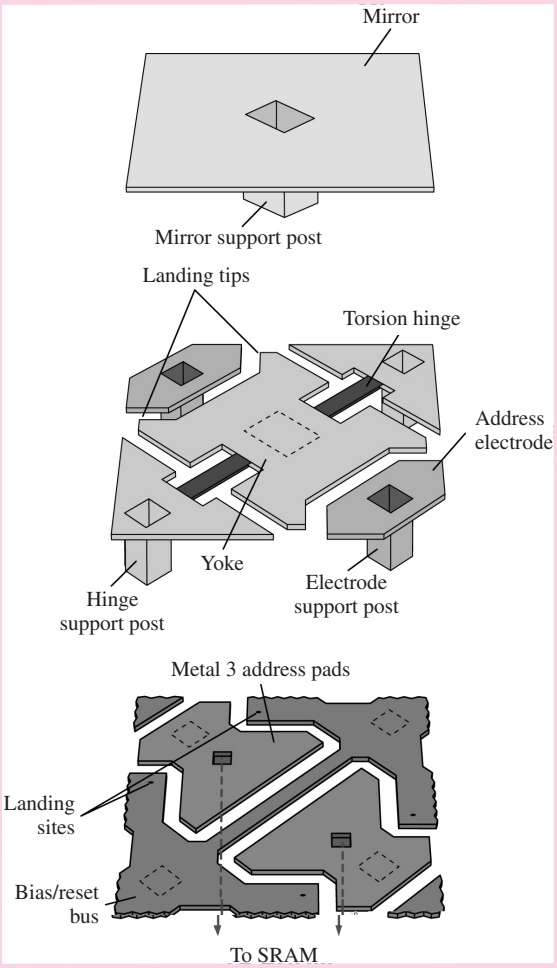
Figure 6.53 Two-input PMOS gates: (a) NOR gate and (b) NAND gate.

Complex logic gates are built up in a manner analogous to the NMOS case. As noted previously, NMOS logic will have a 2.5 × speed advantage over PMOS logic for a given capacitance and power level. The various delay times can be calculated using the formulas presented in Table 6.13.

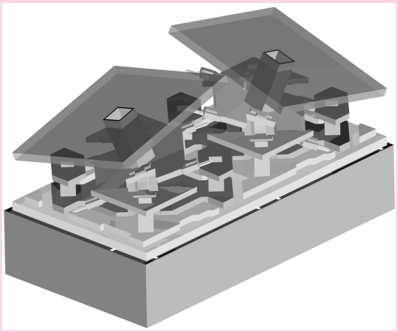
ELECTRONICS IN ACTION

MEMS-Based Computer Projector

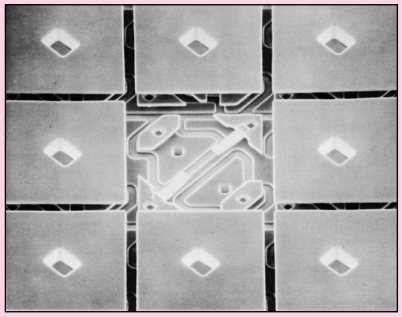
Microelectromechanical systems (MEMS) devices are becoming increasingly important in a variety of applications. MEMS allow one to design mechanical devices controllable by electrical signals and micromachined using tools and techniques similar to those used in the



(a)



(b)



(c)

(a) Details of the micro-mirror pixel structure. (b) Three dimensional view of two adjacent pixels. (c) Magnified view of 9 micro-mirror pixels. The middle mirror and yoke have been removed.

Device photos and drawings are courtesy of Texas Instruments, Inc.

microelectronics industry. MEMS devices are used in applications such as air-bag accelerometers, radio frequency filters, and electrically addressable light modulators.

These figures show a MEMS-based technology developed at Texas Instruments and used at the core of many computer-driven projectors. The device has a large array of 12 to 16 μm mirrors, each of which is controlled by a CMOS SRAM memory cell located underneath each mirror. The mirror rotates about the torsion hinge shown. Depending on the digital value stored in each cell, voltages are driven onto the address electrodes creating electrostatic forces that rotate the mirror into one of two positions. Combined with the appropriate optics, light is directed onto the device and reflected onto a projection screen. Writing appropriate data values in each pixel allows any arbitrary pattern to be created on the screen.

This scheme allows one to turn on or off each pixel. To also include grayscale, the ON time of each pixel is varied by writing different data into the cells during a single display interval. If a mirror is held in the ON position for 20% of a display interval, the human eye will perceive a pixel with an intensity of 20%. Color is created by a sequence of red, green, and blue illumination sources used in rapid sequence to create three sequential color frames. Again, the eye integrates the three color signals and creates the perception of a vast palette of colors. A few projection systems use three separate display chips to create the three-color image frames simultaneously, allowing for greater total optical power to be projected onto very large screens.

The combination of microscale movable mirrors with microelectronics has made possible a new technique for the projection of high resolution and high quality digital images and video. The integration of MEMS and microelectronics is enabling new applications in fields as diverse as medicine, science, transportation, and consumer electronics.

SUMMARY

Chapter 6 introduced a number of concepts and definitions that form a basis for logic gate design. NMOS technology was then used as a vehicle to explore detailed logic circuit design. The geometry of the load device, $(W/L)_L$, is designed to limit the current and power dissipation of the logic gate to the desired level, whereas the geometry of the switching device, $(W/L)_S$, is chosen to provide the desired value of V_L. Transistors are usually designed with either W or L set equal to the minimum feature size achievable in a given technology.

- *Binary logic states:* Binary logic circuits use two voltage levels to represent the Boolean logic variables 1 and 0. In the positive logic convention used throughout this book, the more positive voltage represents a 1, and the more negative level represents a 0. The output of an ideal logic gate would take on only two possible voltage levels: V_H corresponding to the 1 state, and V_L corresponding to the 0 state.
- *Logic state transitions:* The output of the ideal gate would abruptly change state as the input crossed through a fixed reference voltage V_{REF}. However, such an abrupt transition cannot be achieved (it requires infinite gain devices). Logic gates implemented with electronic circuits can only approximate this ideal behavior. The transition between states as the input voltage changes is much more gradual, and a precise reference voltage is not defined. V_{IL} and V_{IH} are defined by the input voltages at which the slope of the voltage transfer

characteristic is equal to -1, and these voltages define the boundaries of the transition region between the logical 1 and 0 levels.

- *Noise margins:* Noise margins are very important in logic gates and represent a measure of the gate's ability to reject extraneous signals. The high-state and low-state noise margins are defined by $\text{NM}_H = V_{OH} - V_{IH}$ and $\text{NM}_L = V_{IL} - V_{OL}$, respectively. Voltages V_{OL} and V_{OH} represent the gate output voltages at the -1 slope points and correspond to the input levels V_{IH} and V_{IL}, respectively. The unwanted signals can be voltages or currents coupled into the circuit from adjacent logic gates, from the power distribution network, or by electromagnetic radiation. The noise margins must also absorb manufacturing process tolerance variations and power supply voltage variations.
- *Logic design goals:* Keep in mind a number of logic gate design goals.
  1. The logic gate should quantize the input signal into two discrete output levels and minimize the width of the undefined input voltage range.
  2. The gate should be unidirectional in nature.
  3. Logic levels must be regenerated as the signal passes through the gate.
  4. Logic gates should have significant fan-in and fan-out capability.
  5. Minimum power and area should be used to meet the speed requirements of the design. Noise margins generally should be as large as possible.
- *Logic delays:* In the time domain, the transition between logic states cannot occur instantaneously. Capacitances exist in any real circuit and slow down the state transitions, thereby degrading the logic signals. Rise time t_r and fall time t_f characterize the time required for a given signal to change between the 0 and 1 or 1 and 0 states, respectively, and the average propagation delay τ_P characterizes the time required for the output of a given gate to respond to changes in its input signals. The propagation delays on the high-to-low (τ_{PHL}) and low-to-high (τ_{PLH}) transitions are typically not equal, and τ_P is equal to the average of these two values.
- *Power-delay product:* The power-delay product PDP, expressed in picojoules (pJ) or femtojoules (fJ), is an important figure of merit for comparing logic families. At low power levels, the power-delay product is a constant, and the propagation delay of a given logic family decreases as power is increased. At intermediate power levels, the propagation delay becomes independent of power level, and at high power levels, the propagation delay of bipolar logic families actually degrades as power is increased.
- *Boolean algebra:* Boolean algebra, developed by G. Boole in the mid-1800s, is a powerful mathematical tool for manipulating binary logic expressions. Basic logic gates provide some combination of the NOT, AND, OR, NAND, or NOR logic functions. A complete logic family must provide at least the NOT function and either the AND or OR functions.
- *Diode and DTL logic:* Simple AND and OR gates can be constructed using diodes, but a transistor must be added to achieve the inversion operation. The combination of a diode AND gate and a bipolar transistor forms a DTL NAND gate.
- *NMOS inverter with resistor load:* Basic inverter design was introduced by considering the static behavior of an inverter using an NMOS switching transistor and a resistor load. Although simple in concept, the resistor is not feasible for use as a load element in ICs because it consumes too much area.
- *IC inverters:* In integrated circuits, the resistor load in the logic gate is replaced with a second MOS transistor, and three possibilities were investigated in detail: the saturated load device, the linear load device, and the depletion-mode load device.
- *Saturated load:* The saturated load device is the most economical configuration because it does not require any modification to the basic MOS fabrication process.

However, saturated load circuits offer the poorest performance in terms of propagation delay.

- *Linear load:* The linear load configuration offers improved performance but requires an additional power supply voltage, which is both expensive and causes substantial wiring congestion in ICs.
- *Depletion-mode load:* Depletion-mode load circuits require additional processing in order to create MOSFETs with a second value to threshold voltage. However, substantial performance improvement can be obtained, and NMOS depletion-mode load technology was the workhorse of the microprocessor industry for many years.
- *NOR and NAND gates:* Multi-input NOR and NAND gates can both easily be implemented in MOS logic. The NOR gate is formed by placing additional transistors in parallel with the switching transistor of the basic inverter, whereas the NAND gate is formed by several switching devices connected in series.
- *Complex logic gates:* An advantage of MOS logic is its ability to implement complex sum-of-products and product-of sums logic equations in a single logic gate, by utilizing both parallel and series connections of the switching transistors. A single load device is required for each logic gate, and one switching transistor is required for each logic input variable.
- *Reference inverter based design:* Once the reference inverter for a logic family is designed, NAND, NOR, and complex gates can all be designed by applying simple scaling rules to the geometry of the reference inverter.
- *MOS body effect:* The influence of the MOSFET body effect cannot be avoided in integrated circuits, and it plays an important role in the design of NMOS (or PMOS) logic gates. Body effect reduces the value of V_H in saturated load logic and generally degrades the current delivery capability of all the load device configurations, thereby increasing the delay of all the logic gates. The MOS body effect has a minor influence on the design of the W/L ratios of the switching transistors in complex logic gates.
- *Rise time, fall time, and propagation delay:* Equations were developed for the rise time, fall time, and propagation delays of the various types of NMOS logic gates, and it was shown that all the time delays of MOS logic circuits are directly proportional to the total equivalent capacitance connected to the output node of the gate. The total effective capacitance is a complicated function of operating point and is due to the capacitance of the interconnections between gates as well as the capacitances of the MOS devices, which include the gate-source (C_{GS}), gate-drain (C_{GD}), drain-bulk (C_{DB}), and source-bulk (C_{SB}) capacitances.
- *Static and dynamic power dissipation:* Power dissipation of a logic gate has a static component and a dynamic component. Dynamic power dissipation is proportional to the switching frequency of the logic gate, the total capacitance, and the square of the logic voltage swing. At low switching frequencies, static power dissipation is most important, but at high switching rates the dynamic component becomes dominant. For a given load capacitance, the power and speed of a logic gate can be changed by proportionately scaling the geometry of the load and switching transistors. For example, doubling the W/L ratios of all devices doubles the power of the gate without changing the static voltage levels of the design. This behavior is characteristic of "ratioed" MOS logic.
- *PMOS logic:* PMOS logic gates are mirror images of the NMOS gates. In order to equal the performance of NMOS, the size of the transistors must be increased in order to compensate for the lower mobility of holes compared to electrons.

KEY TERMS

AND gate
Average propagation delay (τ_p)
Boolean algebra
Complementary MOS (CMOS) technology
Complex logic gates
Depletion load inverter
Diode logic
Diode-transistor logic (DTL)
Dynamic power dissipation
Emitter-coupled logic (ECL)
Fall time t_f
Fan in
Fan out
High logic level at the gate input (V_{IH})
High logic level at the gate output (V_H)
Linear load inverter
Load transistor
Low logic level at the gate input (V_{IL})
Low logic level at the gate output (V_L)
Minimum feature size (F)
MOS device capacitances
NAND gate
Noise margin in high state (NM_H)
Noise margin in low state (NM_L)
NOR gate
On-resistance
OR gate
Output high logic level (V_H)
Output low logic level (V_L)
Power-delay product (PDP)
Power scaling
Propagation delay — high-to-low transition (τ_{PHL})
Propagation delay — low-to-high transition (τ_{PLH})
Ratioed logic
Reference inverter design
Reference voltage (V_{REF})
Resistor load inverter
Rise time t_r
Saturated load inverter
Single-channel technology
Static power dissipation
Sum-of-products logic function
Sum-of-products representation
Switching transistor
Transistor-transistor logic (TTL)
Truth table
V_{OH} — The output voltage corresponding to an input voltage of V_{IL}
V_{OL} — The output voltage corresponding to an input voltage of V_{IH}
Voltage transfer characteristic (VTC)
10 percent point
50 percent point
90 percent point
W/L ratio

REFERENCES

1. J. R. Houser, "Noise margin criteria for digital logic circuits," *IEEE Trans. on Education,* vol. 36, no. 4, pp. 363–368, November 1993.
2. C. F. Hill, "Noise margin and noise immunity in logic circuits," *Microelectronics,* vol. 1, pp. 16–21, April 1968.
3. J. Lohstroh, E. Seevinck, and J. Degroot, "Worst-case static noise margin criteria for logic circuits and their mathematical equivalence," *IEEE J. of Solid-State Circuits,* vol. SC-18, no. 6, pp. 803–806, December 1983.
4. J. D. Meindl and J. A. Davis, "The fundamental limit on binary switching energy for terascale integration (TSI)," *IEEE J. of Solid-State Circuits,* vol. 35, no. 10, pp. 1515–1516, October 2000.
5. R. M. Swanson and J. D. Meindl, "Ion-implanted complementary MOS transistors in low-voltage circuits," *IEEE J. of Solid-State Circuits,* vol. SC-7, no. 2, pp. 146–153, April 1972.
6. G. Boole, *An Investigation of the Laws of Thought, on Which Are Founded the Mathematical Theories of Logic and Probability,* 1849. Reprinted by Dover Publications, Inc., New York: 1954.

ADDITIONAL READING

Nelson, V. P., et al. *Analysis and Design of Logic Circuits*. Prentice-Hall, Englewood Cliffs, N.J.: 1994.

PROBLEMS

Use $K_n' = 25\ \mu A/V^2$, $K_p' = 10\ \mu A/V^2$, $V_{TN} = 1$ V, and $V_{TP} = -1$ V unless otherwise indicated.

General Introduction

6.1. Integrated circuit chips packaged in plastic can typically dissipate only 1 W per chip. Suppose we have an IC design that must fit on one chip and requires 100,000 logic gates. (a) What is the average power that can be dissipated by each logic gate on the chip? (b) If a supply voltage of 5 V is used, how much current can be used by each gate?

6.2. A high-performance microprocessor design requires 10 million logic gates and is placed in a package that can dissipate 40 W. (a) What is the average power that can be dissipated by each logic gate on the chip? (b) If a supply voltage of 3.3 V is used, how much current can be used by each gate? (c) What is the total current required by the IC chip?

6.1–6.2 Ideal Gates, Logic Level Definitions, and Noise Margins

6.3. (a) The ideal inverter in Fig. 6.2(b) has $R = 100\ k\Omega$ and $V_+ = 5$ V. What are V_H and V_L? What is the power dissipation of the gate for $v_O = V_H$ and $v_O = V_L$? (b) Repeat for $V_+ = 3.3$ V.

6.4. Plot a graph of the voltage transfer characteristic for an ideal inverter with $V_+ = 3.3$ V, $V_- = 0$ V, and $V_{REF} = 1.1$ V. Assume $V_H = V_+$ and $V_L = V_-$.

6.5. (a) Plot a graph of the overall voltage transfer function for two cascaded ideal inverters if each individual inverter has a voltage transfer characteristic as defined in Prob. 6.4. (b) What is the overall logic expression $Z = f(A)$ for the two cascaded inverters?

6.6. Plot a graph of the voltage gain A_v of the ideal inverter in Fig. 6.1 as a function of input voltage v_I. ($A_v = dv_O/dv_I$)

6.7. The voltage transfer characteristic for an inverter is given in Fig. 6.54. What are V_H, V_L, V_{IH}, V_{IL}, and the voltage gain A_v of the inverter in the transition region? ($A_v = dv_O/dv_I$)

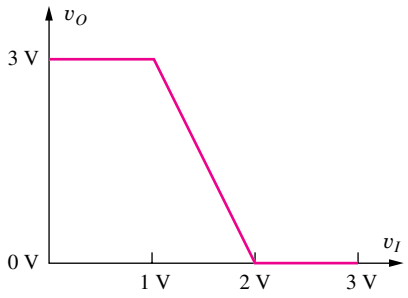


Figure 6.54

6.8. Plot a graph of the overall voltage transfer characteristic for two cascaded inverters if each individual inverter has the voltage transfer function defined in Fig. 6.54.

6.9. Suppose $V_H = 5$ V, $V_L = 0$ V, and $V_{REF} = 2.0$ V for the ideal logic gate in Fig. 6.1. What are the values of V_{IH}, V_{OL}, V_{IL}, V_{OH}, NM_H, and NM_L?

6.10. Suppose $V_H = 3.3$ V and $V_L = 0$ V for the ideal logic gate in Fig. 6.1. Considering noise margins, what would be the best choice of V_{REF}, and why did you make this choice?

6.11. The static voltage transfer characteristic for a practical CMOS inverter is given in Fig. 6.55. What are the values of V_H, V_L, V_{OH}, V_{OL}, V_{IH}, V_{IL}, NM_H, and NM_L?

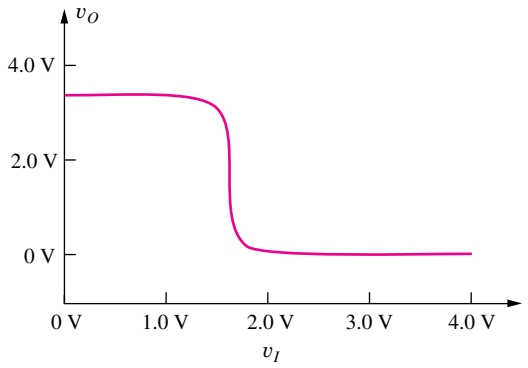


Figure 6.55

6.12. The graph in Fig. 6.56 gives the results of a SPICE simulation of an inverter. What are V_H and V_L for this gate?

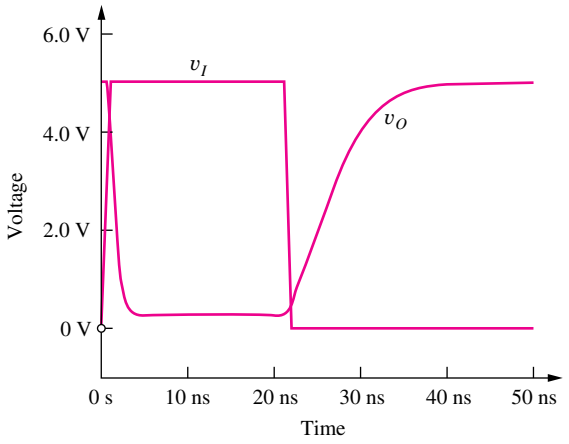


Figure 6.56

6.13. The graph in Fig. 6.57 gives the results of a SPICE simulation of an inverter. What are V_H and V_L for this gate?

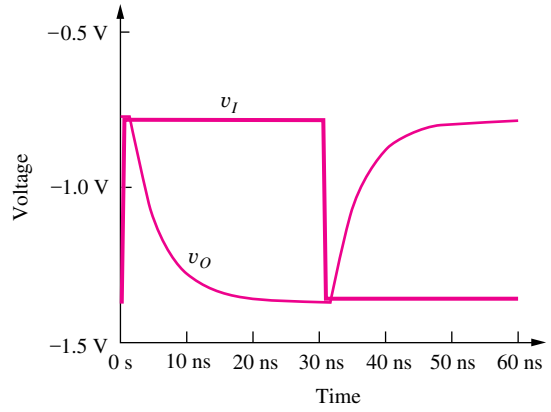


Figure 6.57

6.14. An ECL gate exhibits the following characteristics: $V_{OH} = -0.8$ V, $V_{OL} = -2.0$ V, and $\text{NM}_H = \text{NM}_L = 0.5$ V. What are the values of V_{IH} and V_{IL}?

6.3 Dynamic Response of Logic Gates

6.15. A logic family has a power-delay product of 100 fJ. If a logic gate consumes a power of 100 μW, estimate the propagation delay of the logic gate.

6.16. Integrated circuit chips packaged in plastic can typically dissipate only 1 W per chip. Suppose we have an IC design that must fit on one chip and requires 250,000 logic gates. (a) What is the average power that can be dissipated by each logic gate on the chip? (b) If a supply voltage of 5 V is used, how much current can be used by each gate? (c) If the average gate delay for these circuits must be 2 ns, what is the power-delay product required for the circuits in this design?

6.17. A high-performance microprocessor design requires 8 million logic gates and is placed in a package that can dissipate 40 W. (a) What is the average power that can be dissipated by each logic gate on the chip? (b) If a supply voltage of 3.3 V is used, how much current can be used by each gate? (c) If the average gate delay for these circuits must be 1 ns, what is the power-delay product required for the circuits in this design?

6.18. Plot the power-delay product versus power for the logic gate with the power-delay characteristic depicted in Fig. 6.6.

*6.19. (a) Derive an expression for the rise time of the circuit in Fig. 6.58(a) in terms of the circuit time constant. Assume that $v(t)$ is a 1-V step function, changing state at $t = 0$. (b) Derive a similar expression for the fall time of the capacitor voltage in Fig. 6.58(b) if the capacitor has an initial voltage of 1 V at $t = 0$.

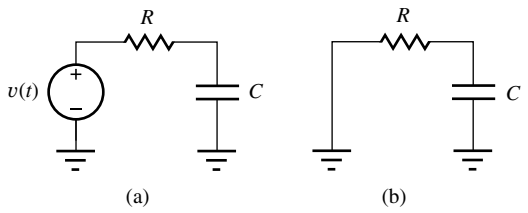


Figure 6.58

6.20. The graph in Fig. 6.56 gives the results of a SPICE simulation of an inverter. (a) What are V_H and V_L for this gate? (b) What are the rise and fall times for v_I and v_O? (c) What are the values of τ_{PHL} and τ_{PLH}? (d) What is the average propagation delay for this gate?

6.21. The graph in Fig. 6.57 gives the results of a SPICE simulation of an inverter. (a) What are V_H and V_L for this gate? (b) What are the rise and fall times for v_I and v_O? (c) What are the values of τ_{PHL} and τ_{PLH}? (d) What is the average propagation delay for this gate?

6.4 Review of Boolean Algebra

6.22. Use the results in Table 6.2 to prove that $(A + B) \cdot (A + C) = A + BC$.

6.23. Use the results in Table 6.2 to simplify the logic expression $Z = AB\overline{C} + ABC + \overline{A}BC$.

6.24. Make a truth table for the expression in Prob. 6.23.

6.25. Use the results in Table 6.2 to simplify the logic expression $Z = \overline{A}\overline{B}C + ABC + \overline{A}BC + A\overline{B}C$.

6.26. Make a truth table for the expression in Prob. 6.25.

6.27. Make a truth table and write an expression for the logic function in Fig. 6.59.

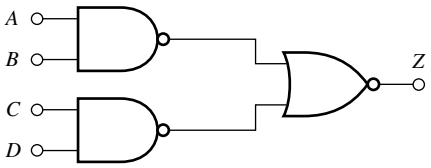


Figure 6.59

6.28. Make a truth table and write an expression for the logic function in Fig. 6.60.

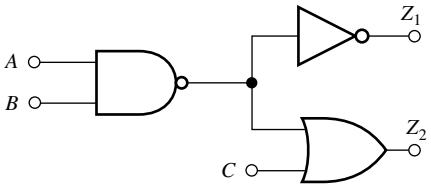


Figure 6.60

6.29. (a) What is the fan out of the NAND gate in Fig. 6.60? (b) Of each NAND gate in Fig. 6.59?

6.5 Diode Logic and DTL

6.30. What logic functions Z are provided by the two circuits in Fig. 6.61?

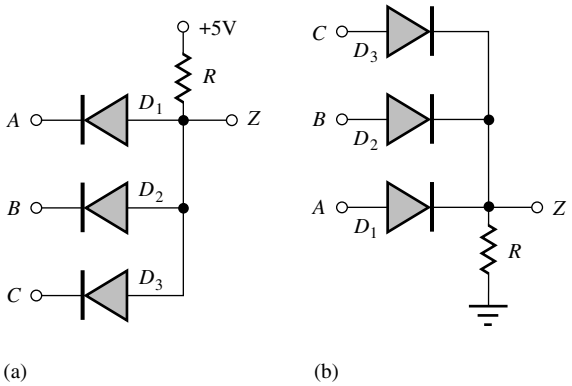


Figure 6.61

6.31. What logic functions Z are provided by the two circuits in Fig. 6.62? Assume the input voltage levels are $1 \equiv 0$ V and $0 \equiv -2$ V.

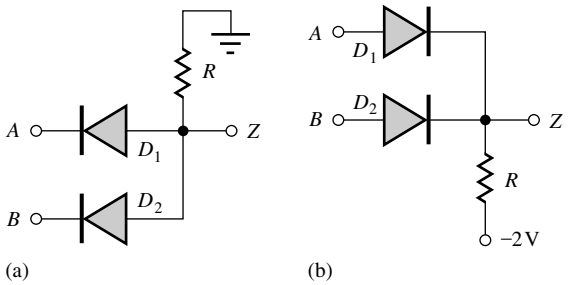


Figure 6.62

6.32. (a) The DTL gate in Fig. 6.13(a) has $R_C = 3$ kΩ, $R_B = 10$ kΩ, and $V_{CESAT} = 0.05$ V. What are the values of the base current I_B and collector current I_C? Is this transistor saturated if $\beta_F = 20$? (b) What is the value of I in Fig. 6.13(b)? (c) What is the power dissipation in the circuit in Fig. 6.13(a)? (d) In Fig. 6.13(b)?

6.33. The DTL gate in Fig. 6.13(a) has $R_C = 3$ kΩ and $R_B = 30$ kΩ. What is the minimum value of β_F for which the transistor is saturated?

6.34. Add a diode to the circuit in Fig. 6.12 to form a three-input DTL NAND gate.

6.35. Two stages of diode logic precede the ideal inverter in Fig. 6.63. What is the expression for the logic output variable $Z = f(A, B, C)$?

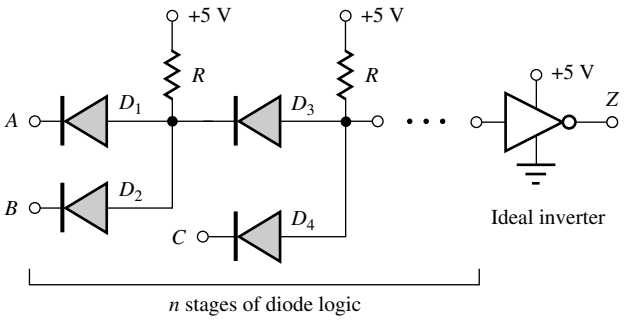


Figure 6.63

*6.36. The ideal inverter in Fig. 6.63 has a reference voltage of 2.5 V. What is the maximum number of diode logic circuits that may be cascaded ahead of the inverter without producing logic errors if the forward voltage of the diode is 0.75 V?

*6.37. Four stages of diode logic circuits are cascaded ahead of the ideal inverter in Fig. 6.63. If the forward voltage of the diodes is 0.70 V, what must be the minimum reference voltage of the inverter if it is to yield valid logic signals at its output?

6.38. Find the base current and calculate the actual saturation voltage of transistor Q_1 in Fig. 6.13(a) using Eq. (5.54) if the collector current is 200 μA, $\beta_F = 60$ and $R_B = 50$ kΩ. Show that I_B and I_C satisfy the conditions needed for saturation. What is the value of R_C?

General Problems

6.39. A high-speed microprocessor must drive a 64-bit data bus in which each line has a capacitive load C of 40 pF, and the logic swing is 3.3 V. The bus drivers must discharge the load capacitance from 3.3 V to 0 V in 1 ns, as depicted in Fig. 6.64. Draw the waveform for the current in the output of the bus driver as a function of time for the indicated waveform. What is the peak current in the microprocessor chip if all 64 drivers are switching simultaneously?

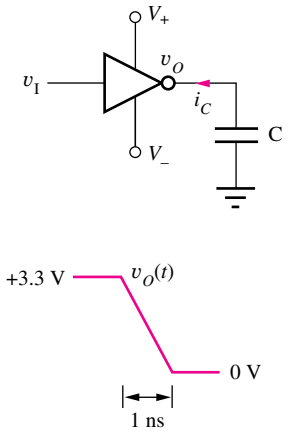


Figure 6.64 Bus driver and switching waveform.

6.40. Repeat Prob. 6.39 for a processor with a 1-GHz clock. Assume that the fall time must be 0.1 ns instead of 1 ns, as depicted in Fig. 6.64.

*6.41. A particular interconnection between two logic gates in an IC chip runs one-half the distance across a 7.5-mm-wide die. The interconnection line is insulated from the substrate by silicon dioxide. If the line is 1.5 μm wide and the oxide ($\varepsilon_{ox} = 3.9\varepsilon_o$ and $\varepsilon_o = 8.85 \times 10^{-14}$ F/cm) beneath the line is 1 μm thick, what is the total capacitance of this line assuming that the capacitance is three times that predicted by the parallel plate capacitance formula? Assume that the silicon beneath the oxide represents a conducting ground plane.

**6.42. Ideal constant-electric-field scaling of a MOS technology reduces all the dimensions and voltages by the same factor α. Assume that the circuit delay ΔT can be estimated from

$$\Delta T = C\frac{\Delta V}{I}$$

in which the capacitance C is proportional to the total gate capacitance of the MOS transistor, $C = C''_{ox}WL$, ΔV is the logic swing, and I is the MOSFET drain current in saturation. Show that constant-field scaling results in a reduction in delay by a factor of α and a reduction in power by a factor of α^2 so that the PDP is reduced by a factor of α^3. Show that the power density actually remains constant under constant-field scaling.

**6.43 For many years, MOS devices were scaled to smaller and smaller dimensions without changing the power supply voltage. Suppose that the width W, length L, and oxide thickness T_{ox} of a MOS transistor are all reduced by a factor of 2. Assume that V_{TN}, v_{GS}, and v_{DS} remain the same. (a) Calculate the ratio of the drain current of the scaled device to that of the original device. (b) By what factor has the power dissipation changed? (c) By what factor has the value of the total gate capacitance changed? (d) By what factor has the circuit delay ΔT changed? (Use the delay formula in Prob. 6.42.)

6.6 NMOS Logic Design

6.44. Integrated circuit chips packaged in plastic DIPs (dual-in-line packages) can typically dissipate 1 W per chip. Suppose that we have an IC design that must fit on one chip and requires 100,000 logic gates. Assume that one-half the logic gates on the chip are conducting current at any given time. (a) What is the average power that can be dissipated by each logic gate on the chip? (b) If a supply voltage of 5 V is used, how much current can be used by each gate?

6.45. A high-performance microprocessor design requires 5 million logic gates and will be placed in a package that can dissipate 20 W. (a) What is the average power that can be dissipated by each logic gate on the chip? (b) If a supply voltage of 3.3 V is

used, how much current can be used by each gate? Assume that two-thirds of the logic gates on the chip are in the conducting state at any given time.

6.46. Design a resistive load inverter to operate from a 2.5-V power supply with a power dissipation of 50 μW. Assume $V_{TN} = 0.60$ V.

6.47. (a) Find V_H, V_L, and the power dissipation (for $v_O = V_L$) for the logic inverter with resistor load in Fig. 6.65(a). (b) Repeat for Fig. 6.65(b).

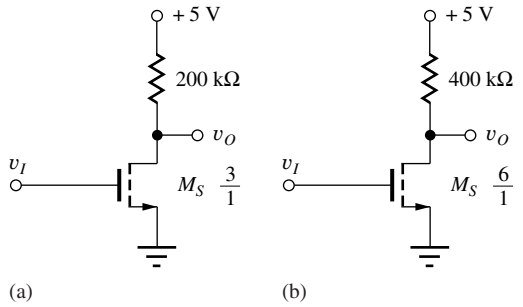


Figure 6.65

6.48. A manufacturing problem caused $V_{TN} = 0.8$ V instead of 1.0 V for the inverter in Fig. 6.65. (a) What are the values of V_H, V_L, and power dissipation? (b) Repeat for $V_{TN} = 1.2$ V.

6.49. (a) What are the noise margins for the circuit in Fig. 6.65(a)? (b) Fig. 6.65(b)?

6.50. (a) Find V_H, V_L, and the power dissipation (for $v_O = V_L$) for the logic inverter with resistor load in Fig. 6.65(b). (b) A manufacturing problem caused $V_{TN} = 0.85$ V instead of 1.0 V. What are the new values of V_H, V_L, and power dissipation? (c) Repeat for $V_{TN} = 1.15$ V.

6.51. (a) What are the noise margins for the circuit in Fig. 6.65(b)? (b) What percentage increase in K_S will result in $N_{ML} = 0$ for the resistive load inverter in Fig. 6.65(b)?

6.52. The resistive load inverter in Fig. 6.16 is to be redesigned for $V_L = 0.5$ V. (a) What are the new values of R and $(W/L)_S$ assuming that the power dissipation remains the same? (b) What are the values of NM_L and NM_H?

6.53. (a) Redesign the resistive load inverter of Fig. 6.16 for operation at a power level of 0.25 mW with $V_{DD} = 3.3$ V. Assume $V_{TO} = 0.7$ V. Keep the other design parameters the same. What is the new size of M_S and the value of R? (b) What are the values for NM_H and NM_L?

6.54. Design an inverter with a resistive load for $V_{DD} = 3$ V and $V_L = 0.25$ V. Assume $I_{DD} = 33$ μA, $K_n' = 60$ μA/V^2, and $V_{TN} = 0.75$ V.

6.55. (a) Design an inverter with a resistive load for $V_{DD} = 2.0$ V and $V_L = 0.15$ V. Assume $I_{DD} = 10$ μA, $K_n' = 75$ μA/V^2, and $V_{TN} = 0.6$ V. (b) Confirm the validity of your design with SPICE.

6.7 Static Design of the NMOS Saturated Load Inverter

6.56. (a) Calculate the on-resistance of an NMOS transistor with $W/L = 10/1$ for $V_{GS} = 5$ V, $V_{SB} = 0$, $V_{TO} = 1$ V, and $V_{DS} = 0$ V. (b) Calculate the on-resistance of a PMOS transistor with $W/L = 10/1$ for $V_{SG} = 5$ V, $V_{SB} = 0$, $V_{TO} = -1$ V, and $V_{SD} = 0$ V. (c) What do we mean when we say that a transistor is "on" even though I_D and $V_{DS} = 0$? (d) What must be the W/L ratios of the NMOS and PMOS transistors if they are to have the same on-resistance as parts (a) and (b) with $|V_{GS}| = 3.0$ V?

6.57. Find V_H for an NMOS logic gate with a saturated load if $V_{TO} = 0.75$ V, $\gamma = 0.75\sqrt{\text{V}}$, $2\phi_F = 0.7$ V, and $V_{DD} = 5$ V.

6.58. Find V_H for an NMOS logic gate with a saturated load if $V_{TO} = 0.6$ V, $\gamma = 0.6\sqrt{\text{V}}$, $2\phi_F = 0.6$ V, and $V_{DD} = 3.3$ V.

6.59. Find V_H for an NMOS logic gate with a saturated load if $V_{TO} = 0.5$ V, $\gamma = 0.85\sqrt{\text{V}}$, $2\phi_F = 0.6$ V, and $V_{DD} = 3$ V.

6.60. Find V_H, V_L, and the power dissipation (for $v_O = V_L$) for the logic inverter with the saturated load in Fig. 6.66. Assume $\gamma = 0$.

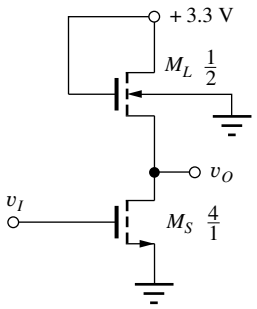


Figure 6.66

6.61. A manufacturing problem caused $V_{TN} = 0.8$ V instead of 1.0 V in the inverter in Fig. 6.66. What are the new values of V_H, V_L, and power dissipation? (c) Repeat for $V_{TN} = 1.2$ V.

*6.62. What are the noise margins for the circuit in Fig. 6.66?

6.63. (a) Find V_H, V_L, and the power dissipation (for $v_o = V_L$) for the logic inverter with the saturated load in Fig. 6.66 if the transistor sizes are changed to $(W/L)_S = 8/1$ and $(W/L)_L = 1/1$. (b) What are the noise margins for the circuit? (c) A manufacturing problem caused $V_{TN} = 0.8$ V instead of 1.0 V. What are the new values of V_H, V_L, and power dissipation?

6.64. The value of K_n' can vary widely due to manufacturing process variations. (a) For the circuit design in Fig. 6.16(b), what value of K_n' will cause N_{MH} to become zero? (b) Repeat for N_{ML}.

6.65. (a) Redesign the saturated load inverter of Fig. 6.26 for operation at a power level of 0.25 mW with $V_{DD} = 3.3$ V. Assume $V_{TO} = 0.7$ V. Keep the other design parameters the same. What are the new sizes of M_L and M_S? (b) What are the new values for NM_H and NM_L?

6.66. Redesign the NMOS logic gate with saturated load of Fig. 6.26 to give $V_L = 0.5$ V and $P = 0.5$ mW for $v_O = V_L$.

6.67. (a) Design a saturated load inverter similar to that of Fig. 6.21(c) with $V_{DD} = 3.3$ V and $V_{OL} = 0.2$ V. Assume $I_{DD} = 33$ μA. (b) Recalculate the values of W/L including body effect, as in Fig. 6.26.

6.68. (a) Design a saturated load inverter similar to that of Fig. 6.26(a) with $V_{DD} = 2.0$ V and $V_L = 0.15$ V. Assume $I_{DD} = 10$ μA and $V_{TN} = 0.6$ V. (b) Recalculate the values of W/L including body effect, as in Fig. 6.32(b) if $V_{TO} = 0.6$ V, $\gamma = 0.6\ \sqrt{\text{V}}$, and $2\phi_F = 0.6$ V. (c) Confirm the validity of your designs with SPICE.

6.69. The logic input of the saturated load inverter of Fig. 6.21(c) is connected to +5 V. What is v_O for this input voltage?

*6.70. The logic input of the saturated load inverter of Fig. 6.26 is connected to +5 V. What is v_O for this input voltage? (This problem will probably require an iterative solution.)

6.71. The saturated load inverter of Fig. 6.32(b) was designed using $K_n' = 25\ \mu\text{A/V}^2$, but due to process variations during fabrication, the value actually turned out to be $K_n' = 18\ \mu\text{A/V}^2$. What will be the new values of V_H, V_L, and the power dissipation in the gate for this new value of K_n'?

6.72. The saturated load inverter of Fig. 6.32(b) was designed using $K_n' = 25\ \mu\text{A/V}^2$, but due to process variations during fabrication, the value actually turned out to be $K_n' = 40\ \mu\text{A/V}^2$. What will be the new values of V_H, V_L, and the power dissipation in the gate for this new value of K_n'?

6.73. Plot the noise margins for the saturated load inverter similar to the design of Fig. 6.32(b) versus $K_R = K_S/K_L$ (see the graph in Fig. 6.31). Note that V_L will be changing.

6.74. Plot the noise margins for the saturated load inverter similar to the design in Ex. 6.5 versus $K_R = K_S/K_L$ (see the graph in Fig. 6.31). Note that V_L will be changing.

6.75. The inverter designs in Fig. 6.32 assume $\lambda = 0$. (a) Does V_H depend upon the value of λ? (b) Use SPICE to find I_{DD} and V_L for the saturated load inverter in Fig. 6.32(b) if $\lambda = 0.02, 0.05$, and $0.1\ \text{V}^{-1}$.

6.8 NMOS Inverter with a Linear Load Device

6.76. Calculate the W/L ratio for the linear load device using the circuit and device parameters that apply to Sec. 6.8, and show that the values presented in Fig. 6.28 are correct.

6.77. What is the minimum value of V_{GG} required for linear region operation of M_L in Fig. 6.32(c) if $V_{TO} = 1$ V, $\gamma = 0.5\ \sqrt{\text{V}}$, and $2\phi_F = 0.6$ V.

6.78. Find V_H, V_L, and the power dissipation (for $v_O = V_{OL}$) for the linear load inverter in Fig. 6.67.

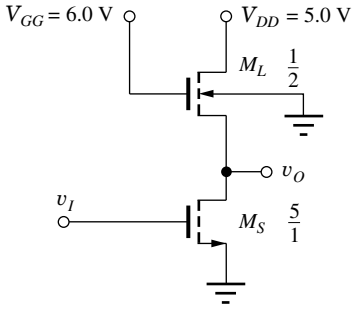


Figure 6.67

6.79. What is the minimum value of V_{GG} in the circuit in Fig. 6.67 if $V_{TO} = 0.6$ V, $\gamma = 0.6\ \sqrt{\text{V}}$, $2\phi_F = 0.6$ V, and $V_{DD} = 3.3$ V?

6.80. (a) Design a linear load inverter similar to that of Fig. 6.67 with $V_{DD} = 3.3$ V, $V_L = 0.20$ V, and $P = 100$ μW. Assume $V_{TO} = 0.6$ V, $\gamma = 0.6\ \sqrt{\text{V}}$, $2\phi_F = 0.6$ V. (b) Confirm the validity of your design using SPICE.

6.9 NMOS Inverter with a Depletion-Mode Load

6.81. We know that body effect deteriorates the behavior of NMOS logic gates with depletion-mode loads. Assume that the depletion-mode load device has $V_{TO} = -3$ V and is operating in an inverter circuit with $V_{DD} = 5$ V. What is the largest value of the body-effect parameter γ that still will allow $V_{OH} = V_{DD}$?

6.82. The depletion load inverter of Fig. 6.32(d) was designed using $K_n' = 25\ \mu A/V^2$, but due to process variations during fabrication, the value actually turned out to be $K_n' = 40\ \mu A/V^2$. What will be the new values of V_H, V_L, and the power dissipation in the gate for this new value of K_n'?

6.83. (a) Redesign the inverter with depletion-mode load of Fig. 6.32(d) for operation with $V_{DD} = 3.3$ V. Assume $V_{TO} = 0.6$ V for the switching transistor and $V_{TO} = -3$ V, $\gamma = 0.5\ \sqrt{V}$, and $2\phi_F = 0.6$ V for the depletion-mode load. Design for $V_L = 0.20$ V and $P = 0.25$ mW. (b) What are the new values for NM_H and NM_L?

6.84. Plot the noise margins for the depletion load inverter described in Prob. 6.82 versus $K_R = K_S/K_L$ (see the graph in Fig. 6.31).

6.85. (a) Design a depletion load inverter to operate with $V_{DD} = 3.3$ V, $V_L = 0.20$ V, and $P = 100\ \mu W$. Assume $V_{TO} = -2$ V, $\gamma = 0.5\ \sqrt{V}$, and $2\phi_F = 0.6$ V for the load transistor and $V_{TO} = 0.6$ V for M_S. (b) Confirm the validity of your design using SPICE.

6.86. The inverter designs in Fig. 6.32 assume $\lambda = 0$. (a) Does V_H depend upon the value of λ? (b) Use SPICE to find I_{DD} and V_L for the depletion-load inverter in Fig. 6.32(d) if $\lambda = 0.02$, 0.05, and 0.1 V^{-1}.

6.11 NMOS NAND and NOR Gates

6.87. (a) What is the value of V_L in the two-input NOR gate in Fig. 6.33(a) when both $A = 1$ and $B = 1$? (b) What is the current in V_{DD} for this input condition?

6.88. Calculate the W/L ratios of the switching devices in the NAND gate in Fig. 6.35(b) and verify that they are correct.

**6.89. The two-input NAND gate in Fig. 6.35 was designed with equal values of R_{on} (approximately equal voltage drops) in the two series-connected switching transistors, but an infinite number of other choices are possible. Show that the equal R_{on} design requires the minimum total gate area for the switching transistors.

6.90. Draw the schematic for a four-input NOR gate with a saturated load device. What are the W/L ratios of all the transistors, based on the reference inverter in Fig. 6.32?

6.91. Draw the schematic for a four-input NAND gate with a depletion-mode load device. What are the W/L ratios of all the transistors, based on the reference inverter in Fig. 6.32?

6.92. Draw the layout of a two-input NOR gate similar to that in Fig. 6.37(a) but use a saturated load device. Be sure to scale the transistor sizes properly based on Fig. 6.32(b).

6.93. (a) Draw the layout of a three-input NOR gate similar to that in Fig. 6.37(a). Be sure to scale the transistor sizes properly. (b) Draw the layout of a three-input NAND gate similar to that in Fig. 6.37(b). Be sure to scale the transistor sizes properly.

6.12 Complex NMOS Logic

6.94. (a) What is the logic function that is implemented by the gate in Fig. 6.68? (b) What are the W/L ratios for the transistors, based on the reference inverter design of Fig. 6.32(d)?

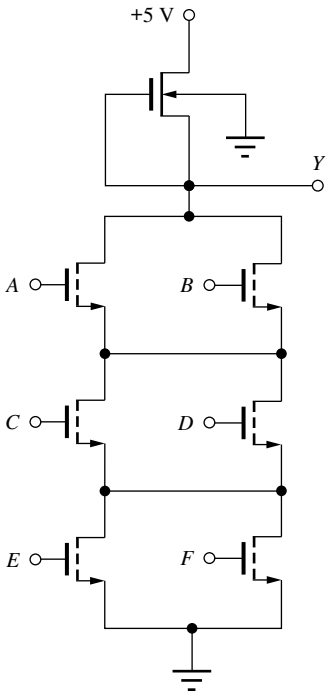


Figure 6.68

6.95. (a) Redraw the circuit in Fig. 6.68 using a saturated load transistor. (b) What is the logic function of the new circuit? (c) What are the W/L ratios of the transistors based upon the reference inverter design in Fig. 6.32(b)?

6.96. (a) What is the logic function that is implemented by the gate in Fig. 6.69? (b) What are the W/L ratios for the transistors, based on the reference inverter design of Fig. 6.32(d)?

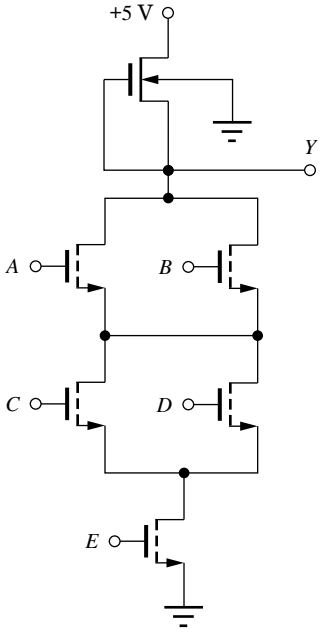


Figure 6.69

6.97. (a) Redraw the circuit in Fig. 6.69 using a saturated load transistor. (b) What is the logic function of the new circuit? (c) What are the W/L ratios of the transistors based upon the reference inverter design in Fig. 6.32(b)?

6.98. (a) What is the logic function that is implemented by the gate in Fig. 6.70? (b) What are the W/L ratios for the transistors if the gate is to dissipate three times as much power as the reference inverter design of Fig. 6.32(d)?

6.99. (a) Redraw the circuit in Fig. 6.70 using a saturated load transistor. (b) What is the logic function of the new circuit? (c) What are the W/L ratios of the transistors based on the reference inverter design in Fig. 6.32(b)?

6.100. Design a depletion-load gate that implements the logic function $Y = \overline{A[B + C(D + E)]}$, based on the reference inverter design of Fig. 6.32(d).

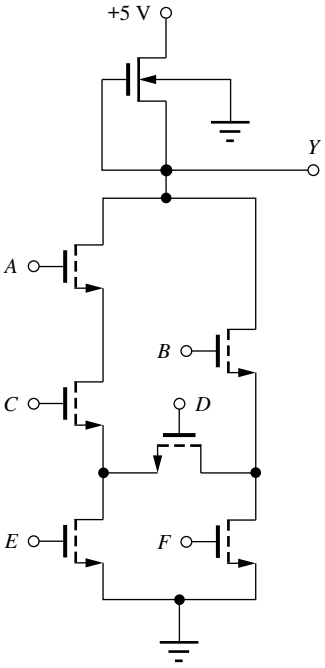


Figure 6.70

6.101. Design a depletion-load gate that implements the logic function $Y = \overline{A(BC + DE)}$ and consumes one-half the power of the reference inverter design of Fig. 6.32(d).

6.102. Design a saturated-load gate that implements the logic function $Y = \overline{A(BC + DE)}$, based on the reference inverter design of Fig. 6.32(b).

6.103. Design a saturated-load gate that implements the logic function $Y = \overline{A(B + CD) + E}$, based on the reference inverter design of Fig. 6.32(b).

6.104. What is the logic function for the gate in Fig. 6.71? What are the W/L ratios of the transistors that form the gate if the gate is to consume twice as much power as the reference inverter in Fig. 6.32(d)?

6.105. (a) Design a depletion-load gate that implements the logic function $Y + \overline{A(B + CD) + E}$, based on the reference inverter design of Fig. 6.32(d). (b) Redesign the W/L ratios of this gate to account for body effect and differences in values of V_{DS} for the various transistors.

6.106. Recalculate the W/L ratios of the transistors in the gate in Fig. 6.37 to account for the body effect and differences in the V_{DS} of the various transistors.

*6.107. Recalculate the W/L ratios of the transistors in the gate in Fig. 6.38(a) to account for the body

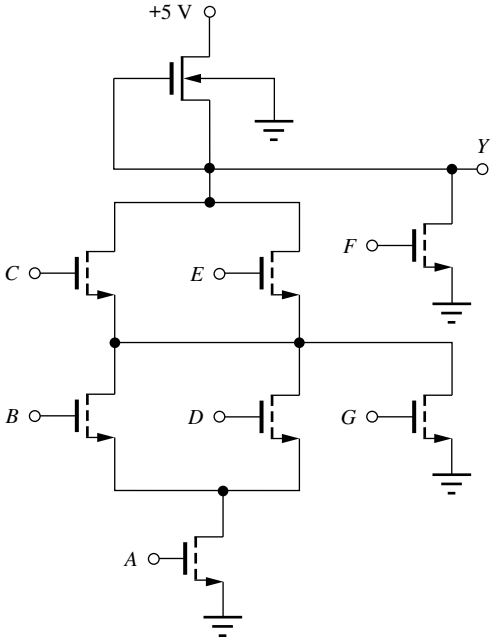


Figure 6.71

effect and differences in the V_{DS} of the various transistors.

*6.108. Recalculate the W/L ratios of the transistors in the gate in Fig. 6.38(b) to account for the body effect and differences in the V_{DS} of the various transistors.

*6.109. Recalculate the W/L ratios of the transistors in the gate in Fig. 6.39 to account for the body effect and differences in the V_{DS} of the various transistors.

*6.110. A new logic gate design is presented in Fig. 6.72. Find V_H and V_L for this design. (*Hint:* For V_L, note that the drain currents of M_S and M_L must be equal, one device will be operating in the triode region, and one will be operating in the saturation region.)

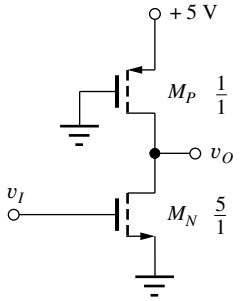


Figure 6.72

**6.111. (a) What is the truth table for the logic function Y for the gate in Fig. 6.73? (b) Write an expression for the logical output of this gate. (c) What are the sizes of the transistors M_S and M_P in order for $V_{OL} \leq 0.25$ V? (d) Qualitatively describe how the sizes of M_S and M_P will change if body effect is included in the models for the transistors. (e) What is the name for this logic function?

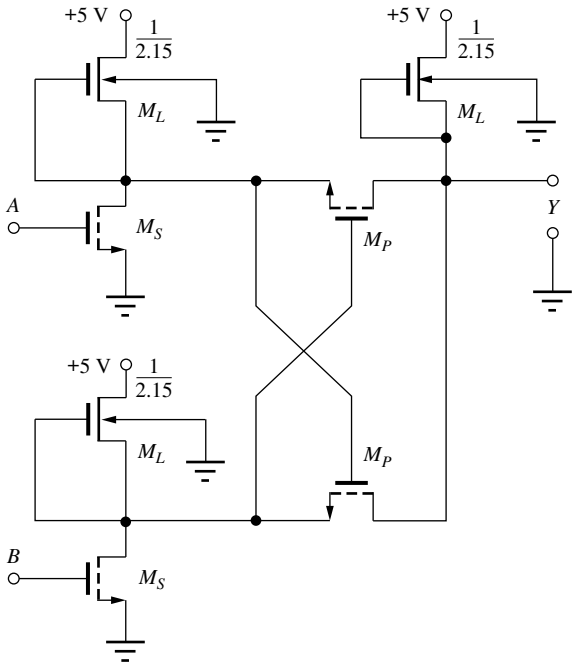


Figure 6.73

6.13 Power Dissipation

6.112. Scale the sizes of the resistors and transistors in the four inverters in Fig. 6.32 to change the power dissipation level to 1 mW.

6.113. What are the W/L ratios of the transistors in the gate in Fig. 6.71 if the gate is to consume four times as much power as the reference inverter in Fig. 6.32(d)?

6.114. What are the W/L ratios for the transistors in Fig. 6.68 if the gate is to dissipate one-quarter as much power as the reference inverter design of Fig. 6.32(d)?

6.115. (a) Scale the transistor sizes in Fig. 6.38(a) to increase the gate power by a factor of three. (b) Scale the transistor sizes in Fig. 6.38(a) to decrease the gate power by a factor of five.

6.116. (a) Scale the transistor sizes in Fig. 6.38(b) to decrease the gate power by a factor of 10. (b) Scale the transistor sizes in Fig. 6.38(b) to increase the gate power by a factor of 2.5.

6.117. (a) Scale the transistor sizes in Fig. 6.39 to quadruple the gate power. (b) Scale the transistor sizes in Fig. 6.39 to decrease the gate power by a factor of three.

*6.118. For many years, MOS devices were scaled to smaller and smaller dimensions without changing the power supply voltage. Suppose that the width W, length L, and oxide thickness t_{ox} are all reduced by a factor of 2. Assume that V_{TN}, v_{GS}, and v_{DS} remain the same. Calculate the ratio of the drain current of the scaled device to that of the original device. How has the power dissipation changed?

6.119. A high-speed NMOS microprocessor has a 64-bit address bus and performs a memory access every 50 ns. Assume that all address bits change during every memory access, and that each bus line represents a load of 10 pF. (a) How much power is being dissipated by the circuits that are driving these signals if the power supply is 5 V? (b) 3.3 V?

6.14 Dynamic Behavior of MOS Logic Gates

**6.120. The capacitive load on a logic gate becomes dominated by the channel capacitance as the transistors are made wider and wider. Assume that W is very large and show that τ_{PHL} and τ_{PLH} become independent of W and are both proportional to (L^2/μ), where L is the channel length. This result shows the importance of achieving as small a channel length as possible.

6.121. A logic family has a power-delay product of 100 fJ. If a logic gate consumes a power of 100 μW, what is the expected propagation delay of the logic gate?

6.122. The graph in Fig. 6.74 gives the results of a SPICE simulation of an inverter. (a) What are the rise and fall times for v_I and v_O? (b) What are the values of τ_{PHL} and τ_{PLH}? (c) What is the average propagation delay for this gate?

6.123. One method to estimate the average propagation delay of an inverter is to construct a long ring of inverters, as shown in the Fig. 6.75. This circuit is called a *ring oscillator,* and the output of any inverter in the chain will be similar to a square wave. (a) Suppose that the chain contains 301 inverters and the average propagation delay of an inverter is 100 ps. What will be the period of the square wave generated by the oscillator? (b) Why should the number of inverters be odd? What could happen if an even number of inverters were used in the ring oscillator?

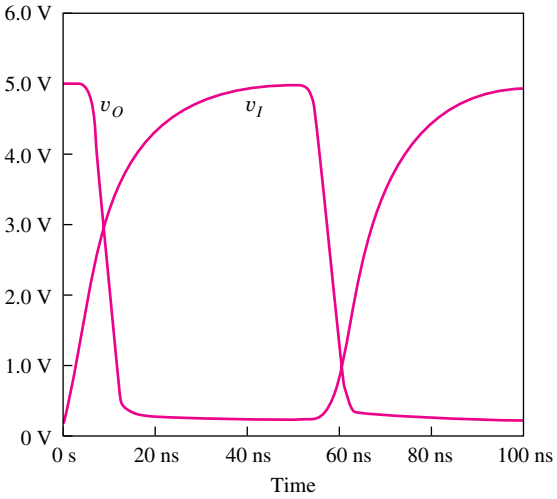


Figure 6.74

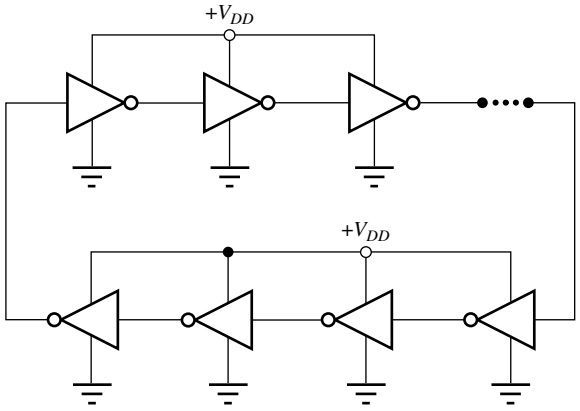


Figure 6.75 Ring oscillator formed from a chain of an *odd* number of inverters.

Resistor Load

6.124. What are the rise time, fall time, and average propagation delay of the NMOS gate in Fig. 6.16(b) if a load capacitance $C = 0.5$ pF is attached to the output of the gate?

6.125. What are the rise time, fall time, and average propagation delay of the NMOS gate in Fig. 6.16(b) if a load capacitance $C = 0.5$ pF is attached to the output of the gate and V_{DD} is reduced to 3.3 V?

6.126. Design an NMOS inverter with resistor load ($V_{DD} = 5$ V, $V_L = 0.25$ V) to have an average propagation delay of 2.5 ns with a capacitive load of 1 pF. What is the average static power dissipation of this gate?

6.127. Repeat the simulation of Ex. 6.11 with $\lambda = 0.04$/V. Compare the new values rise time, fall time, and propagation delays with those of the example.

Saturated Load

6.128. What are the rise and fall times and average propagation delays of the NMOS gate in Fig. 6.76 if $C = 0.5$ pF and $V_{DD} = 5$ V?

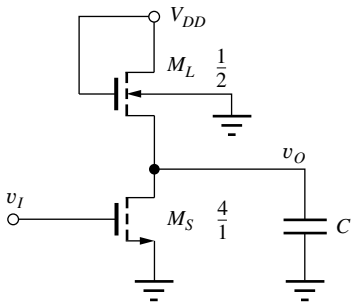


Figure 6.76

6.129. What are the rise and fall times and average propagation delays of the NMOS gate in Fig. 6.76 if $C = 0.3$ pF and $V_{DD} = 3.3$ V?

6.130. Design an NMOS saturated load inverter ($V_{DD} = 5$ V, $V_L = 0.25$ V) to have an average propagation delay of 2 ns with a capacitive load of 1 pF. What is the average static power dissipation of this gate?

6.131. Repeat the simulation in Ex. 6.12 with $\lambda = 0.04$/V. Compare the new values rise time, fall time, and propagation delays with those of the example.

6.132. Use SPICE to determine the characteristics of the NMOS inverter with a saturated load device for the design given in Fig. 6.32(b). (a) Simulate the voltage transfer function. (b) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} for this inverter with a square wave input and $C = 0.25$ pF. Compare your results to the formulas developed in the text.

**6.133. Use SPICE to simulate the behavior of a chain of five saturated load inverters from Fig. 6.32(b). The input to the first inverter should be a square wave with 0.1-ns rise and fall times and a period of 100 ns. (a) Calculate t_r, t_f, τ_{PHL}, and τ_{PLH} using the input and output waveforms from the first inverter in the chain, and compare your results to the formulas developed in the text. What value of C [Fig. 6.42(b)] did you use? (b) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} from the waveforms at the input and output of the fourth inverter in the chain, and compare your results to the formulas developed in the text. What value of C [Fig. 6.42(b)] did you use? (c) Discuss the differences between the results in (a) and (b).

Linear Load

6.134. Use SPICE to determine the characteristics of the NMOS inverter with a linear load device for the design given in Fig. 6.32. (a) Simulate the voltage transfer function. (b) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} for this inverter with a square wave input and $C = 0.15$ pF.

**6.135. Use SPICE to simulate the behavior of a chain of five linear load inverters from Fig. 6.32. The input to the first inverter should be a square wave with 0.1-ns rise and fall times and a period of 100 ns. (a) Calculate t_r, t_f, τ_{PHL}, and τ_{PLH} using the input and output waveforms from the first inverter in the chain. (b) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} from the waveforms at the input and output of the fourth inverter in the chain. (c) Discuss the differences between the results in (a) and (b).

Depletion-Mode Load

6.136. What are the sizes of the transistors in the NMOS depletion-mode load inverter if it must drive a 1-pF capacitance with an average propagation delay of 3 ns? Assume $V_{DD} = 3.0$ V and $V_L = 0.25$ V. What are the rise and fall times for the inverter? Use $V_{TNL} = -3$ V ($\gamma = 0$).

6.137. Design an NMOS depletion load inverter ($V_{DD} = 3.3$ V, $V_L = 0.20$ V, $V_{TNS} = 0.75$ V, $V_{TNL} = -2$ V, $\gamma = 0$) to have an average propagation delay of 1 ns with a capacitive load of 0.2 pF. What is the average static power dissipation of this gate?

6.138. Repeat the simulation in Ex. 6.13 with $\lambda = 0.04$/V. Compare the new values rise time, fall time, and propagation delays with those of the example.

6.139. Use SPICE to determine the characteristics of the NMOS inverter with a depletion-mode load device for the design given in Fig. 6.32(d). (a) Simulate the voltage transfer function. (b) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} for this inverter with a square wave input and $C = 0.2$ pF. Compare your results to the formulas developed in the text.

**6.140. Use SPICE to simulate the behavior of a chain of five depletion-mode load inverters from Fig. 6.32(d). The input to the first inverter should be a square wave with 0.1-ns rise and fall times and a period of 100 ns. (a) Calculate t_r, t_f, τ_{PHL}, and τ_{PLH} using the input and output waveforms from the first inverter in the chain, and compare your results to the formulas developed in the text. What value of C [Fig. 6.42(b)] did you use? (b) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} from the waveforms at the input and output of the fourth inverter in the chain, and compare your results to the formulas developed in the text. (c) Discuss the differences between the results in (a) and (b).

**6.141. Use SPICE to determine the characteristics of the two-input NMOS NAND gate with a depletion-mode load device for the design given in Fig. 6.35(b). (a) Simulate the voltage transfer function by varying the voltage at input A with the voltage at input B fixed at 5 V. (b) Repeat the simulation in (a), but now vary the voltage at input B with the voltage at input A fixed at 5 V. Plot the results from (a) and (b) and note any differences. (c) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} for this inverter with a square wave input at input A with the voltage at input B fixed at 5 V. (d) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} for this inverter with a square wave input at input B with the voltage at input A fixed at 5 V. (e) Compare the results from (c) and (d). (f) Determine t_r, t_f, τ_{PHL}, and τ_{PLH} for this inverter with a single square wave input applied to both inputs A and B. Compare the results to those in (c) and (d).

6.15 A Final Comparison of Load Devices

6.142. Currents in the various load devices are shown in Fig. 6.49. The resistor load has a value of 95 kΩ. The W/L ratios of the devices were chosen to set the current in each load device to 50 μA when $v_O = V_L = 0.25$ V. Calculate the values of the W/L ratios of the load devices that were used in the figure for the: (a) saturated load device including body effect, (b) saturated load device with no body effect, (c) linear load device including body effect, (d) linear load device with no body effect, (e) depletion-mode load device including body effect, (f) depletion-mode load with no body effect.

6.143. Create a table similar to Table 6.14 for a technology with $V_{DD} = 3.3$ V, $V_L = 0.25$ V, $V_{TNS} = 0.75$ V, and $V_{TNL} = -2$ V.

6.144. Create a table similar to Table 6.14 for a technology with $V_{DD} = 2.5$ V, $V_L = 0.20$ V, $V_{TNS} = 0.60$ V, and $V_{TNL} = -1.5$ V.

6.16 PMOS Problems

6.145. Design four PMOS logic gates similar to the ones in Fig. 6.32. Do not do a complete mathematical redesign, but design the PMOS circuits by scaling the W/L ratios in Fig. 6.32, assuming that $K'_p = 10\ \mu A/V^2$.

*6.146. What are the values of V_L and V_H for the inverter in Fig. 6.77?

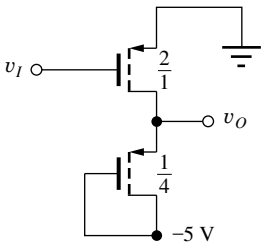


Figure 6.77

6.147. Calculate the noise margins for the circuit in Fig. 6.77.

6.148. Design the transistors in the inverter of Fig. 6.78 so that $V_H = -0.33$ V and the power dissipation = 0.1 mW. Use the values in Table 6.8 on page 386, except $V_{TO} = -0.7$ V and $K'_p = 10\ \mu A/V^2$.

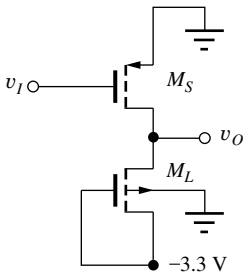


Figure 6.78

*6.149. What are the noise margins for the circuit in Prob. 6.148?

6.150. What are the values of V_H and V_L for the inverter of Fig. 6.79? Use the values in Table 6.8 on page 386, except $V_{TO} = -1$ V and $K'_p = 10\ \mu A/V^2$.

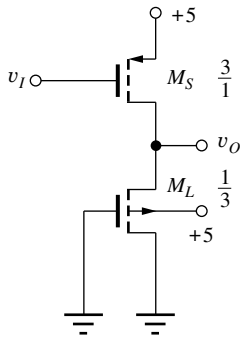


Figure 6.79

6.151. What is the logic function Y for the gate in Fig. 6.80?

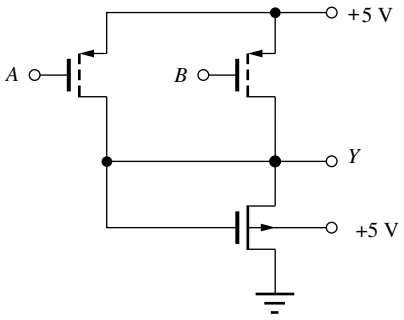


Figure 6.80

6.152. What is the logic function Y for the gate in Fig. 6.81?

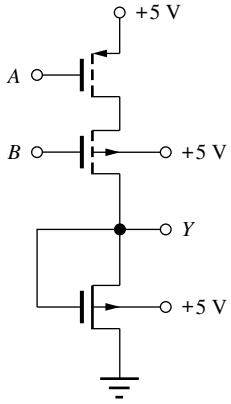


Figure 6.81

6.153. Simulate the voltage transfer characteristic for the PMOS gate in Fig. 6.77, and compare the results to those of Prob. 6.146.

6.154. Simulate the voltage transfer characteristic for the PMOS gate in Fig. 6.78, and compare the results to those of Prob. 6.148.

6.155. Simulate the voltage transfer characteristic for the PMOS gate in Fig. 6.79, and compare the results to those of Prob. 6.150.

6.156. Simulate the delay of the PMOS gate in Fig. 6.77 with a load capacitance of 1 pF, and determine the rise time, fall time, and average propagation delay.

6.157. Simulate the delay of the PMOS gate in Fig. 6.79 with a load capacitance of 1 pF, and determine the rise time, fall time, and average propagation delay.